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MS-AA51

Version 1.01

CPU:

Intel Conroe (65W Dual core)

System Chipset:

Intel G41 - MCH (North Bridge)

Intel ICH7 (South Bridge)

On Board Chipset:

BIOS -- SPI

HD --ALC887

AMP --TI2008

LPC Super I/O -- F71808LAB

LAN-- REALTEK RTL8111E

CLOCK -- RTM875-605

CARDREADER -- RTS5159

Main Memory:

DDR III SO-DIMM*2 (Max 4GB)

Expansion Slots:

MINI-PCIE X1 SLOT*2

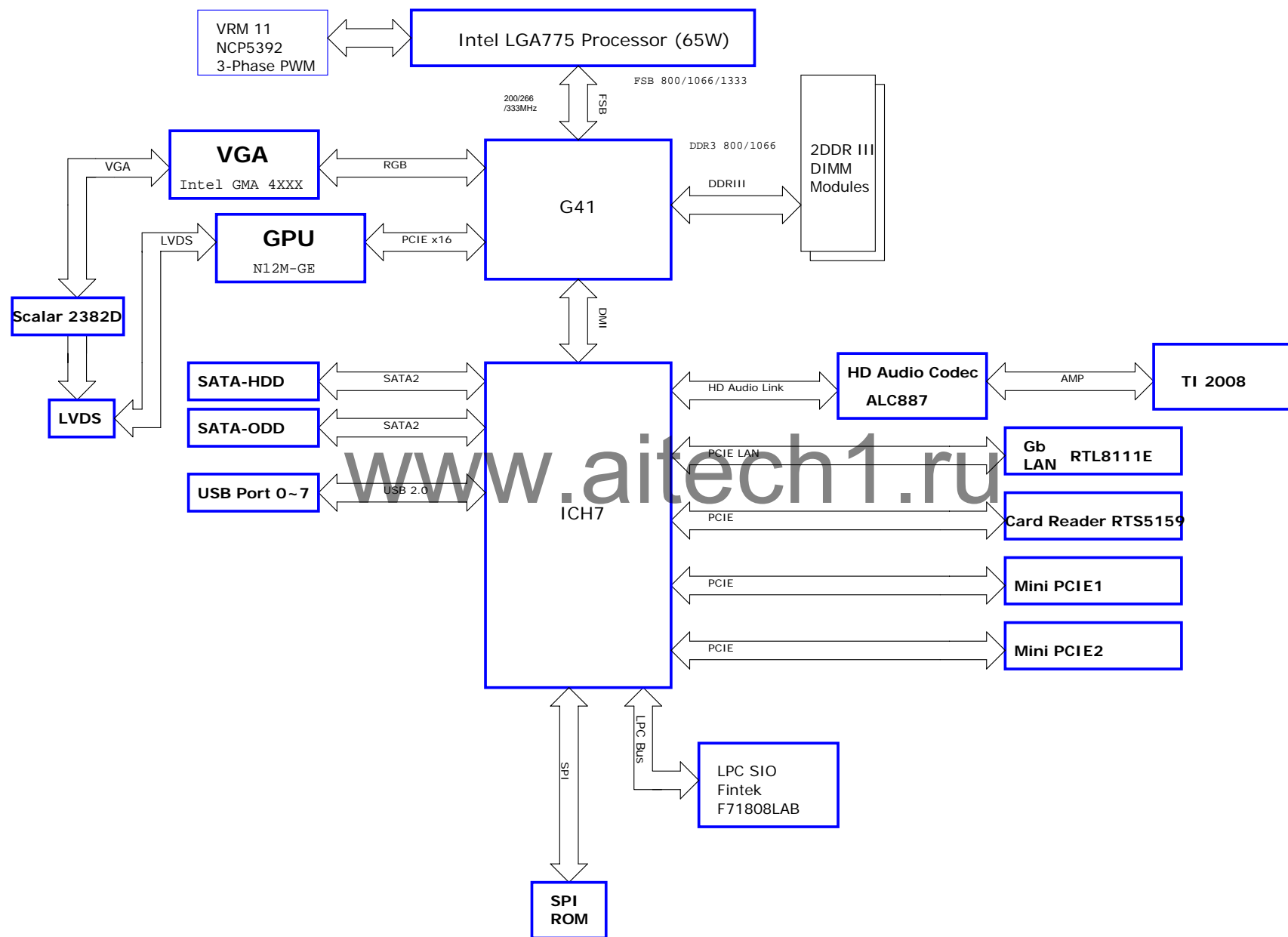
NCP5392 PWM

Controller: 3 PHASES

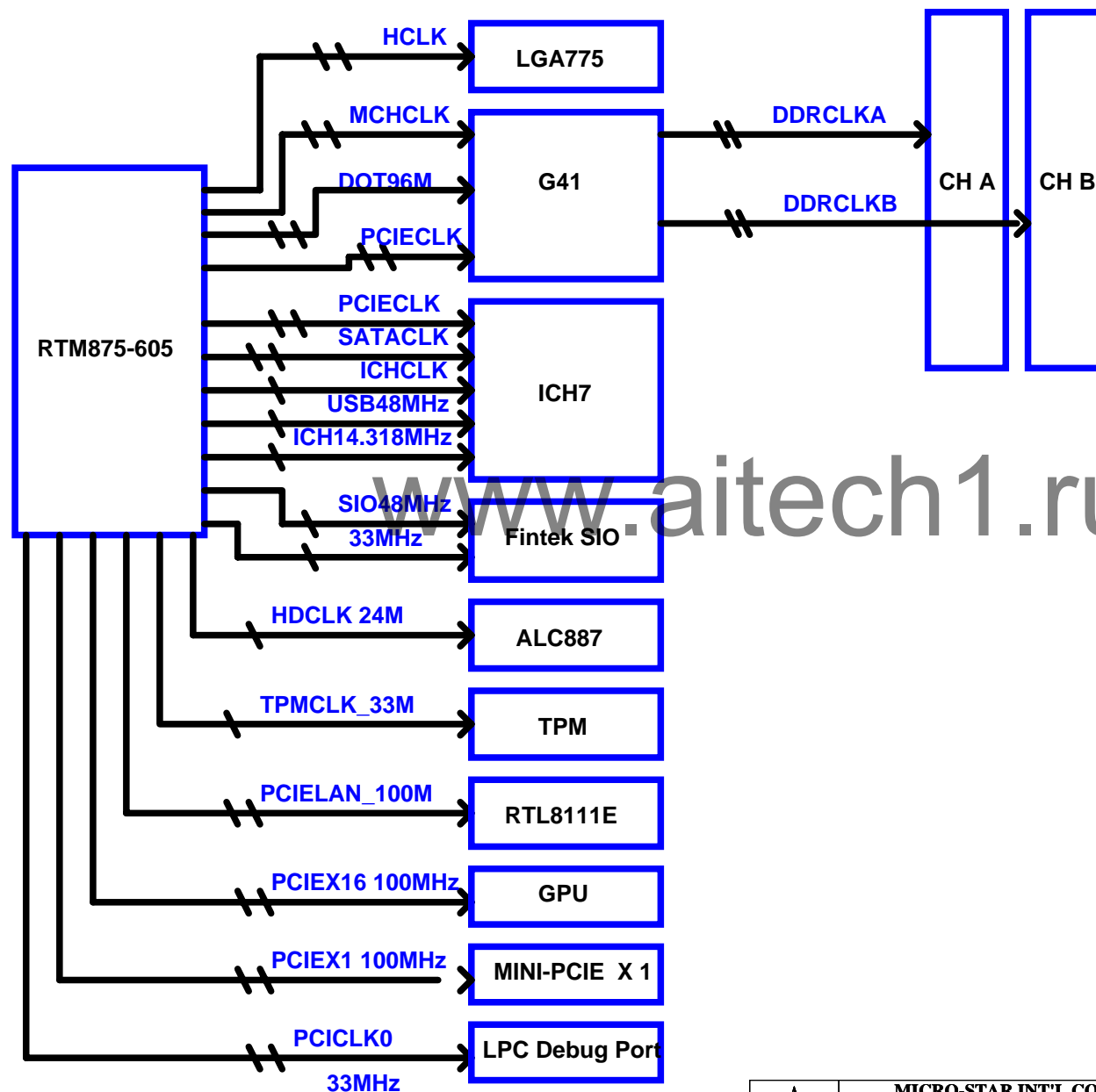
GPU

N12M

Block Diagram



CLOCK MAP



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Size Custom	Document Description CLOCK MAP	Rev 1.01
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LGA775 - CPU (65W)		
1.15V-1.50V Core	-	75A
1.2V FSB VTT	-	4.6A

G41		
1.2V FSB_VTT	-	1.0A
1.1V Core	-	18.25A
1.1V DMI/PCI Exp.	-	1.345A
1.5V VCC_DDR (S0,S1)	-	1.963A
1.5V VCC_SMCLK	-	288mA
3.3V VCCA_DAC	-	65.8mA
3.3V VCC33	-	15.8mA
1.1V Vcc CL	-	4.06A

ICH7		
1.05V Core	-	1.31A
1.5V DMI	-	40 mA
1.2V FSB_VTT	-	14 mA
1.5V_A USB/SATA	-	0.97A
1.5V_B PCI Exp.	-	0.74A
VCCRTC	-	6 uA
3.3V CL	-	12 mA
1.5V GbE LAN	-	74 mA
3.3V 10/100 LAN	-	12 mA
3.3V GbE LAN	-	1 mA
3.3V SusHDA	-	4 mA
3.3V HDA	-	24 mA
3.3V VccSus3_3	-	700mA
3.3V Vcc3_3	-	580mA

HD Audio ALC887		
3.3V AUDIO	-	48mA
5V AUDIO	-	200mA

RTM875-605		
3.3V VDD_48/PCI/REF	-	0.25A

REALTEK/RTL8111DL		
3.3V_SB I/O & LED	-	70mA

3V
Battery

INTERSIL 6333		
VCCP VRM 11	-	4.8A
1.15V-1.50V	-	75A
3-Phase Switch	-	75A

+1.0VRUN Regulator		
+1.0VRUN	-	2.52A
1.05V Linear	-	2.5A

uP7711U8		
VTT_DDR	-	1.2A
0.75V Linear	-	1.2A

VCC_DDR Regulator		
VCC_DDR 1.5V PWM	-	4.7A
4.7A+3.7A+9.36A+4.5A+5A	-	27.26A

V_1P1_CORE Regulator		
V_1P1_CORE	-	1.4A
1.1V PWM	-	24A

+1.8V_REG Regulator		
+1.8V_REG	-	0.22A
1.8V Linear	-	1.475A

V_FSB_VTT Regulator		
V_FSB_VTT	-	4.56A
1.2V Linear	-	5.7A

V_1P5_ICH Regulator		
V_1P5_ICH	-	2A
1.05V Linear	-	4.8A

V_1P05_ICH Regulator		
V_1P05_ICH	-	0.92A
1.5V Linear	-	1.4A

TI/TPS51125			
5VSB	5.2A	VCC5	5.1A
		VCC3	2.35A
		3VSB	2A+2A=4A

+19V
ADAPTER

DDRII x2 & TERMINATOR		
0.75V VTT_DDR	-	1.2A
1.5V VCC_DDR (S0,S1)	-	4.7A
1.5V VCC_DDR (S3)	-	400mA

GPU		
+1.05VRUN	-	2.45A
+3VRUN_VGA	-	0.6A
VDDR(1.5V)	-	5A
NVDD_CORE(1V)	-	18A
+1.8V_REG	-	0.22A

Mini PCI-E slot x2		
3VSB	-	1A
1.5V	-	2A

FINTEK SIO 71808LAB		
VCC3	-	10mA

USB x8		
+5V (S0,S1)	-	4A
+5V (S3)	-	30mA

+12V SYS & N12M FAN		
	-	2A

+8V - 0.5A		
	-	0.5A

Cardreader RTS159		
VCC3	-	50mA

AMP2008		
	-	1.8A

INVERTER		
	-	2.5A

DSUB&SATA&ODD		
	-	2.2A

SATA HDD		
	-	1A

+12V		
	-	1A

LCD_VDD		
	-	1.1A

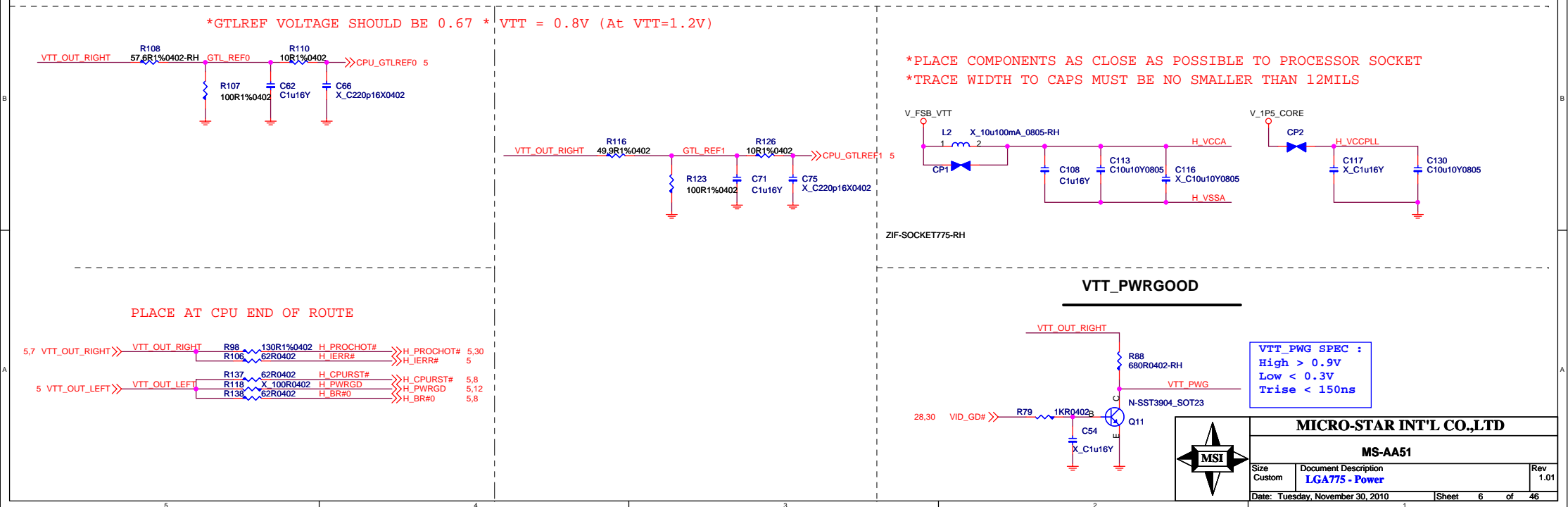
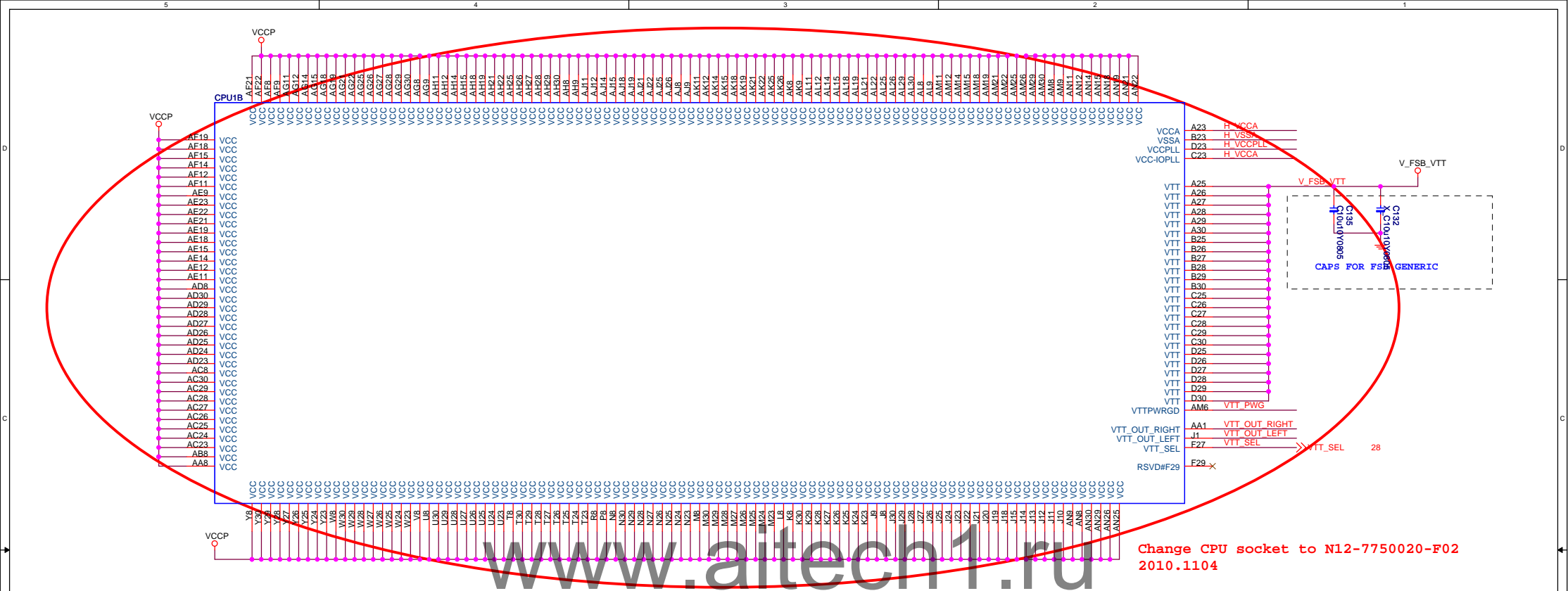
+12V ON Semi/NCP1587DR2G		
2A+0.5A+1A+2.5A	-	6A

CPU SIGNAL BLOCK

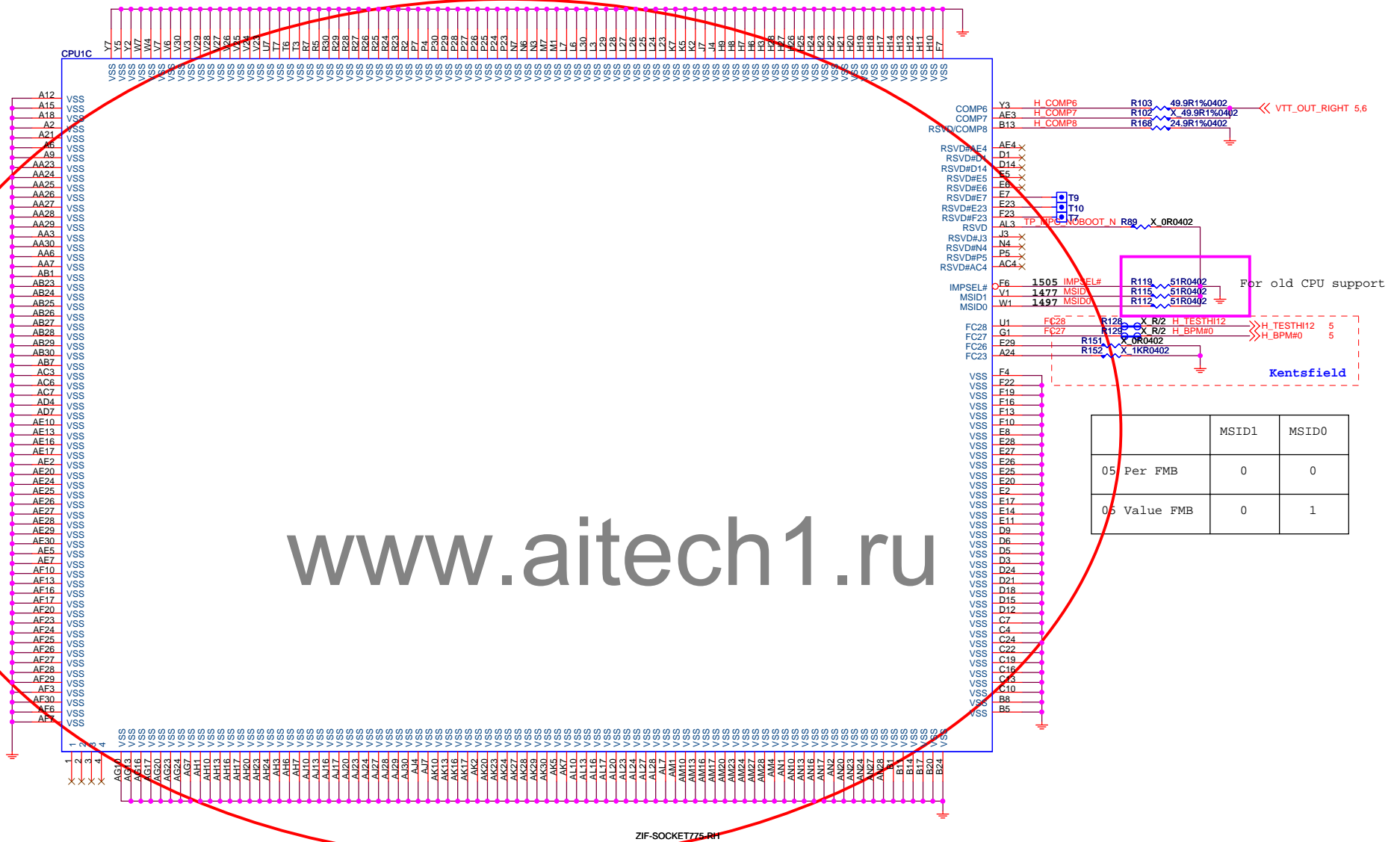


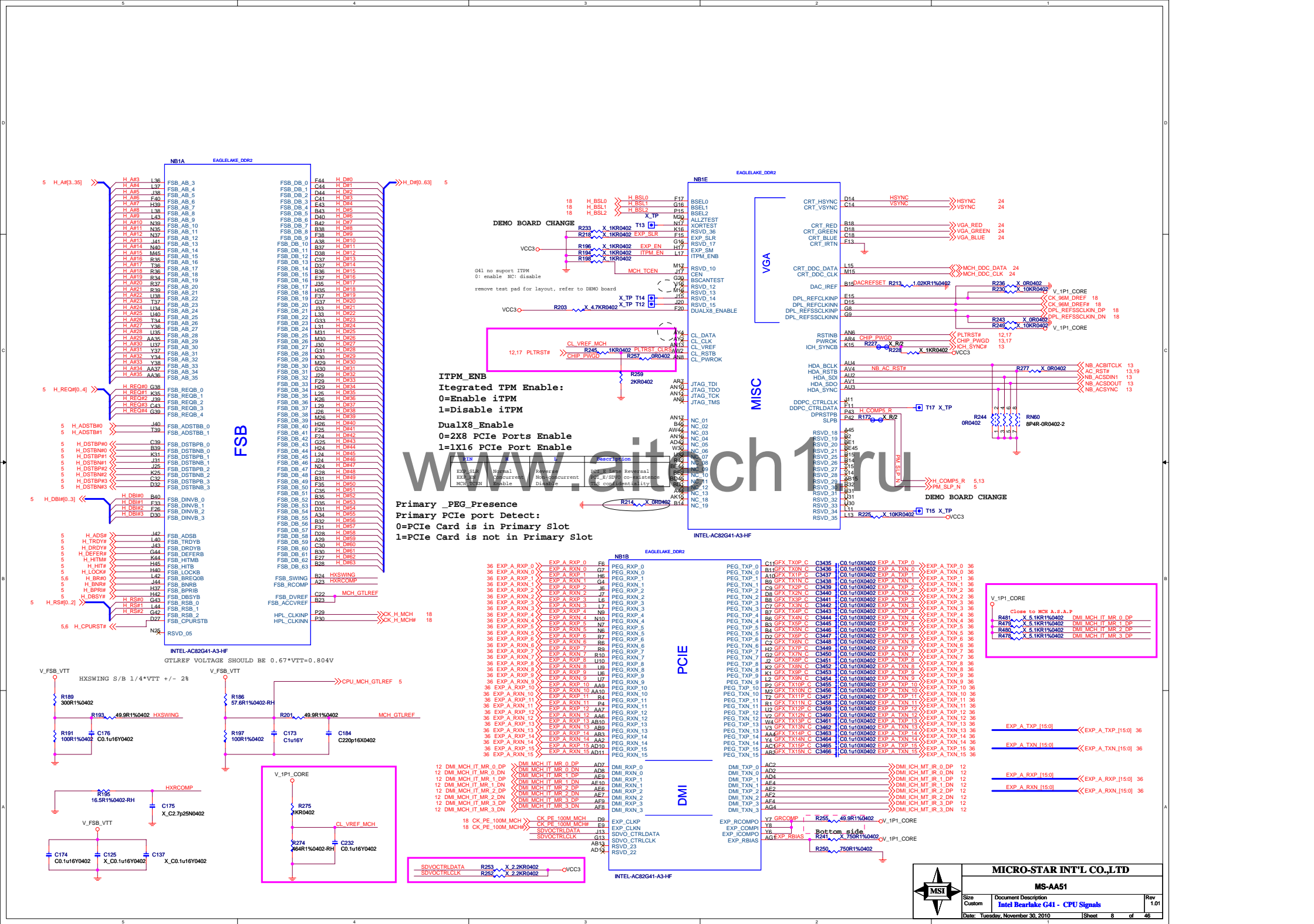
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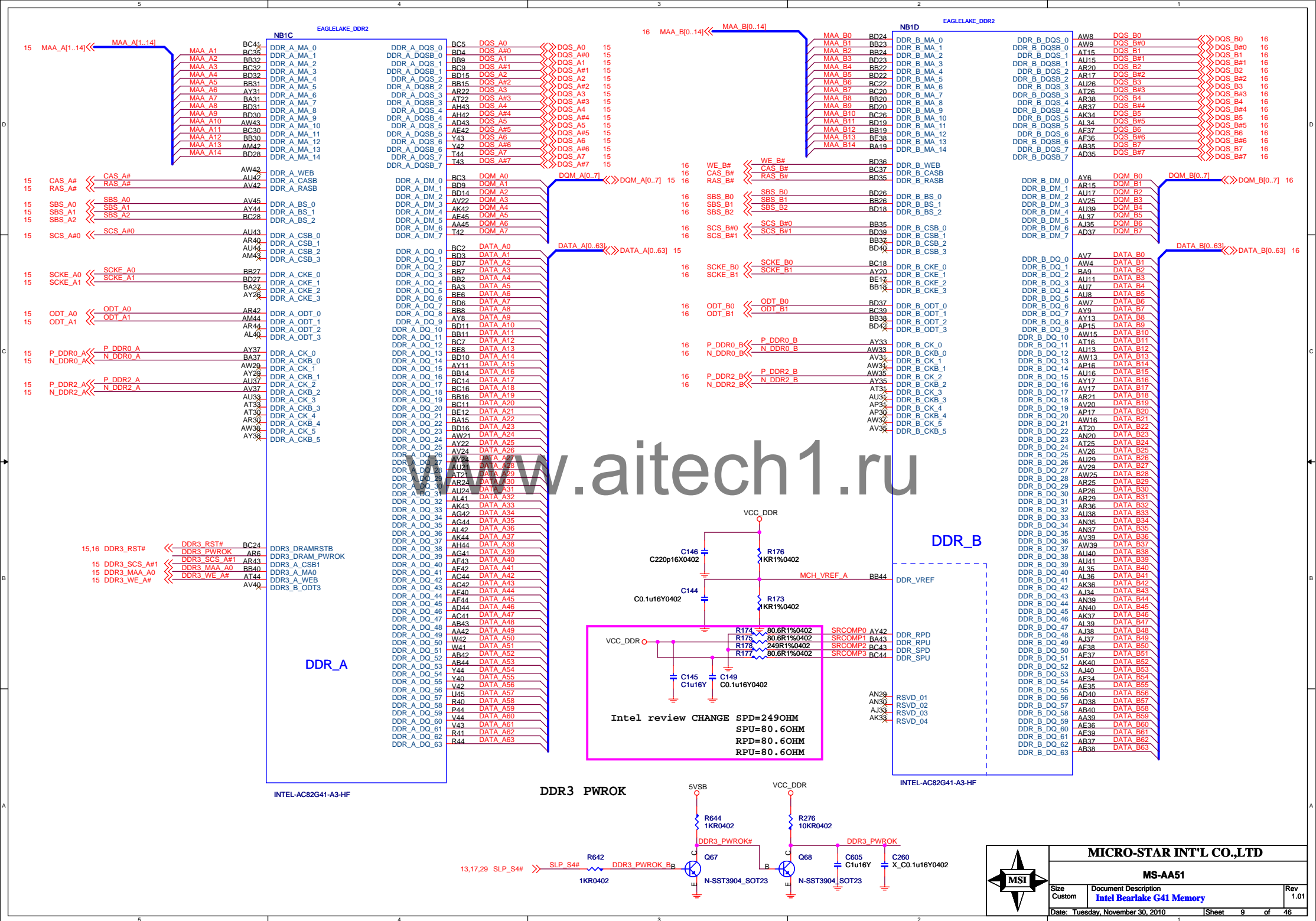
Kentsfield

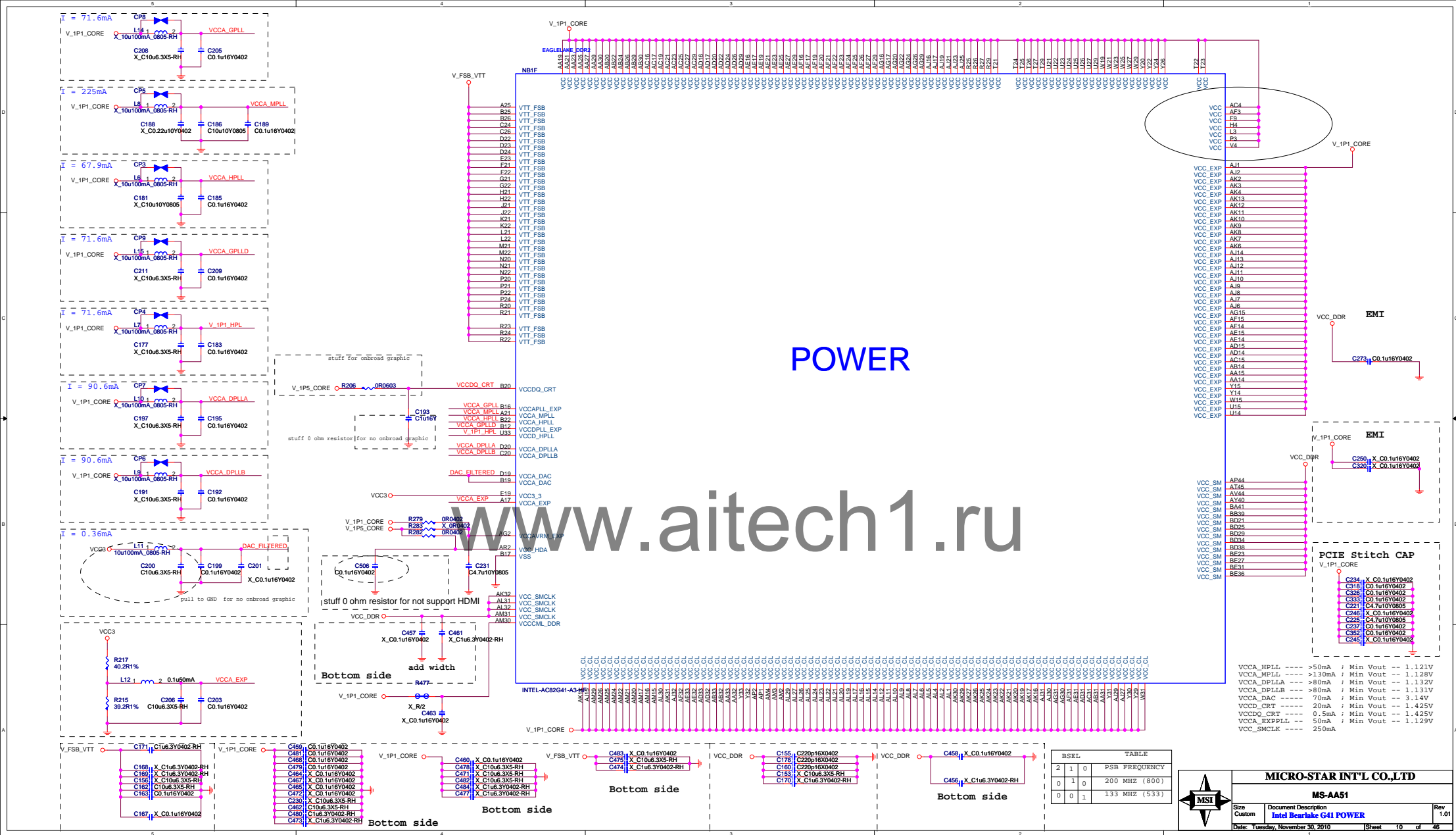


Change CPU socket to N12-7750020-F02
2010.1104









NB1G



N8
N38
N36
N33
N30
N29
N26
N16
N13
N11
M44
M25
M24
M1
L9
L8
L4
L39
L36
L30
L26
L20
L16
L10
K45
K33
K29
K24
K20
K17
K13
K11
J9
J8
J5
J4
J37
J3
J9
H8
H7
H44
H38
H33
H31
H30
H25
H20
H16
H15
H13
H11
H1
G35
G3
G29
G26
G24
G17
G11
F9
F45
F42
F4
F30
F2
F16
E5
E41
E31
E3
D7
D6
D39
D26
D25
D21
D16
D11
C5
C3
BE40
BE34
BE29
BE25
BE21
BE19
BE15
BE10
BD8
BD17
BD12
AD30
AC30
AE30
AE30



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Size
CustomDocument Description
Intel Bearlake G41 GNDRev
1.01

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GNT5#	GNT4#	ROUTING
0	1	Flash Cycles Routed to SPI
1	0	Flash Cycles Routed to PCI
1	1	Flash Cycles Routed to LPC

8P4R change to single resistor 2010.1103

PCI INTERFACE

ICH 7
PART 1/3

PCI EXPRESS

DIRECT MEDIA

LAN

INTERRUPT SPI

SPI FLASH ROM

SPI DEBUG PROT
Close to SPI ROM

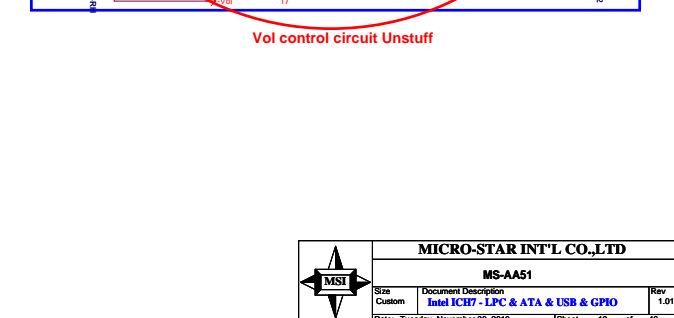
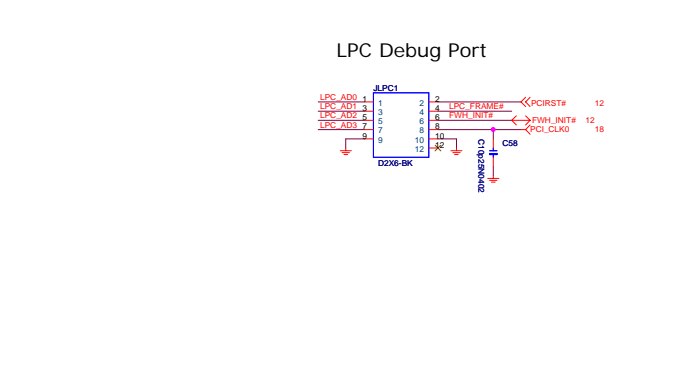
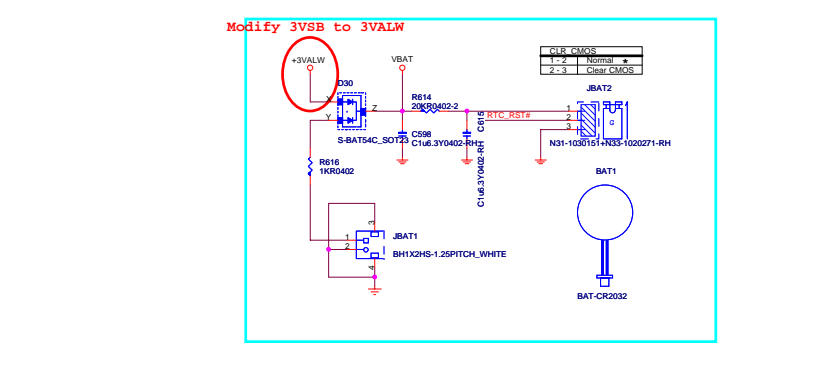
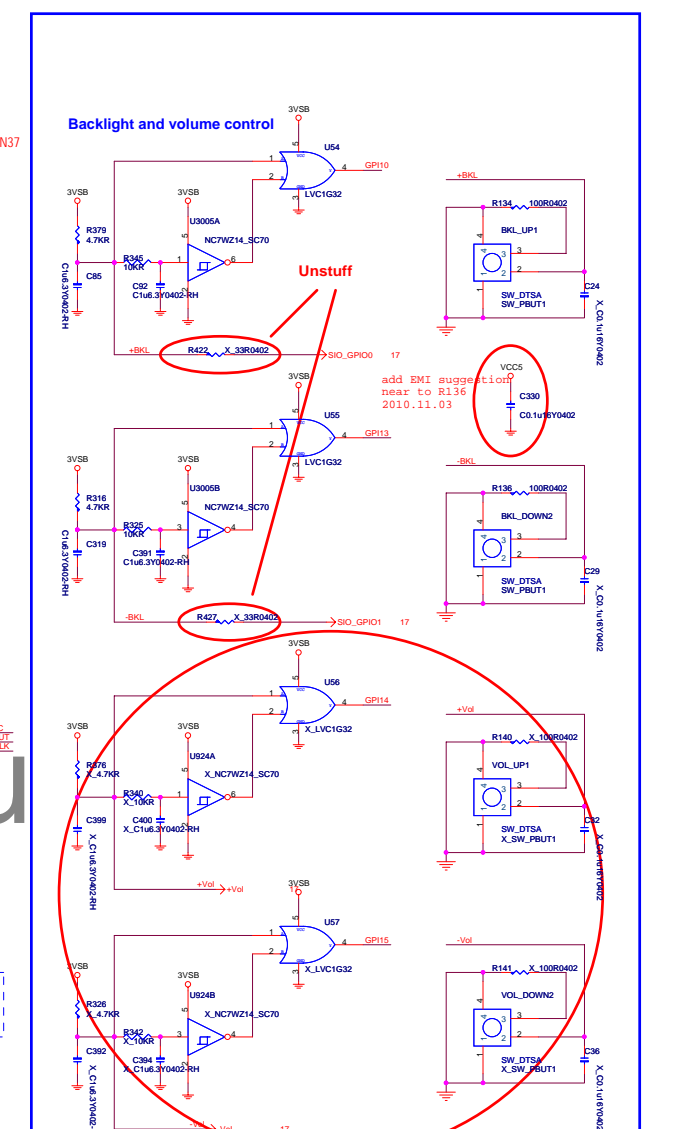
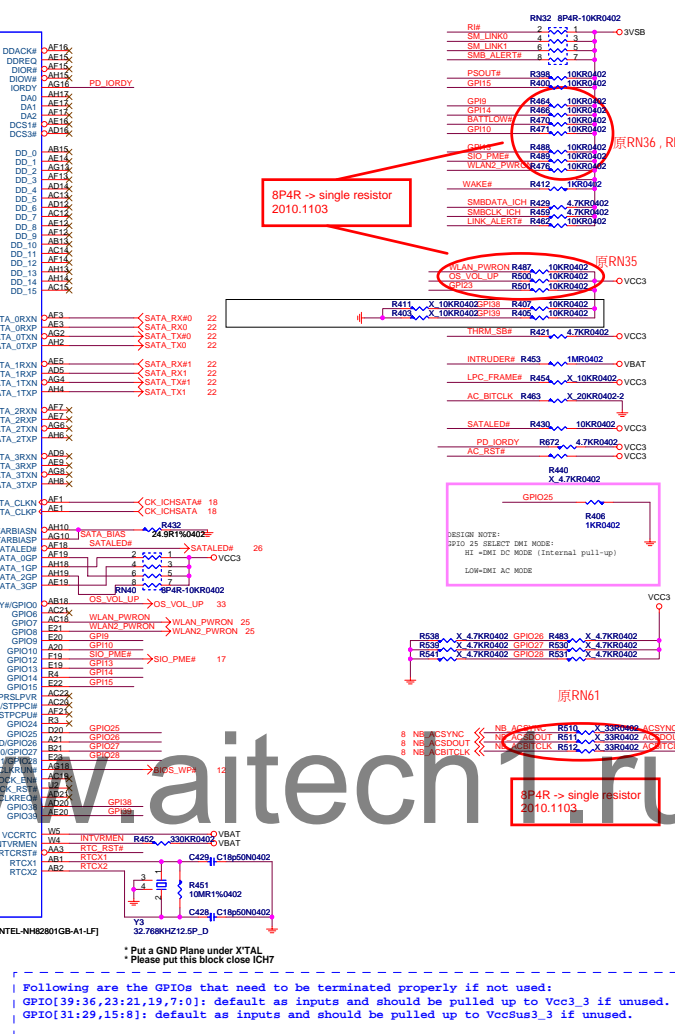
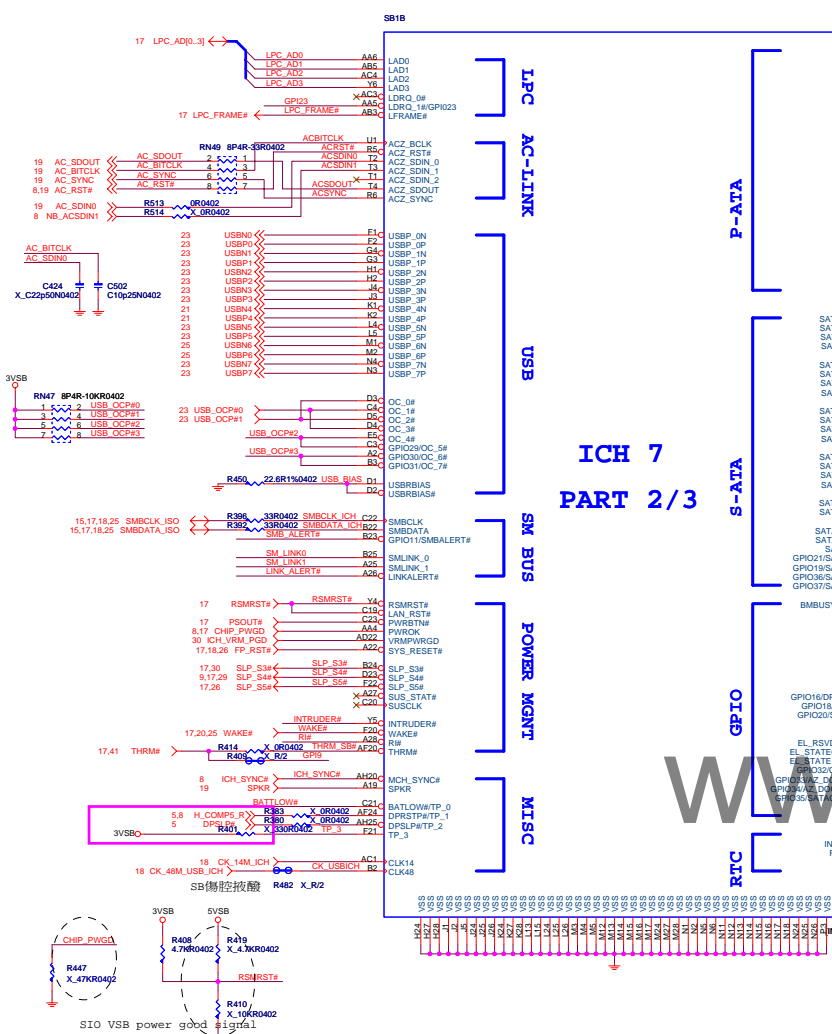


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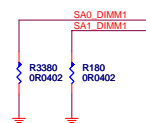
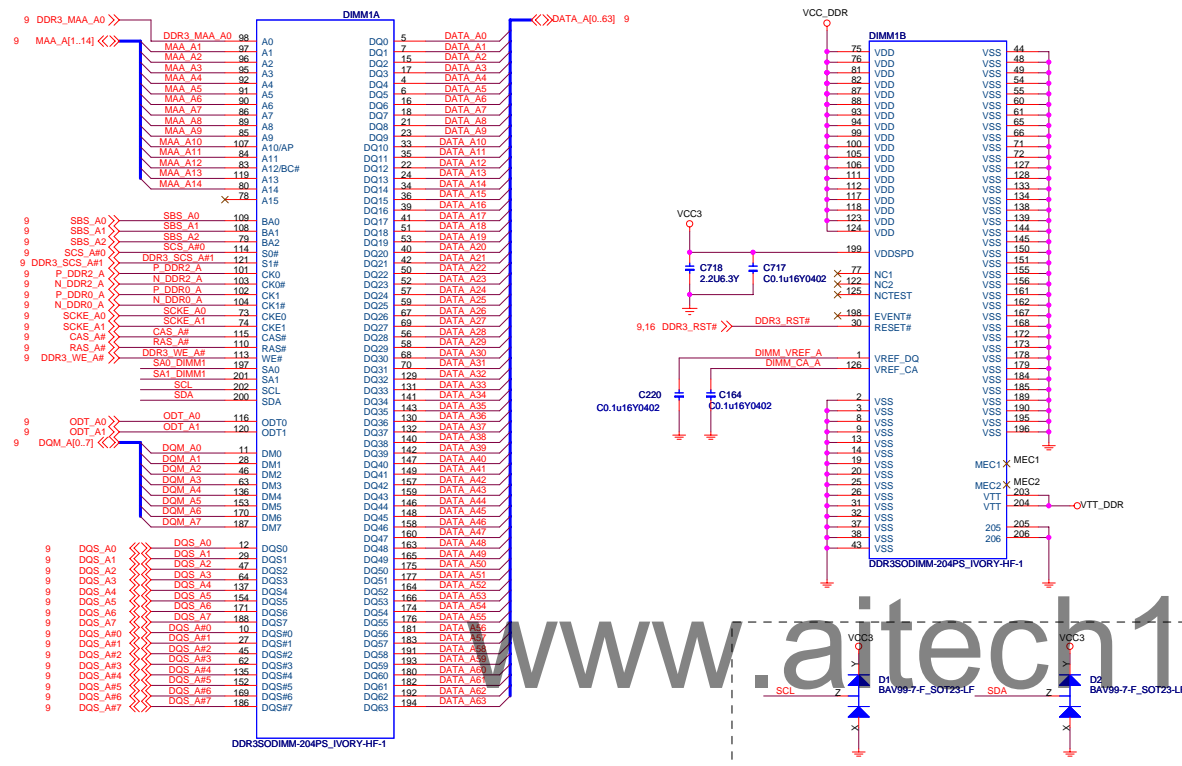
MS-AA51

Size	Document Description	Rev
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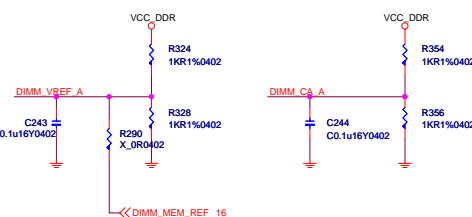
Date: Tuesday, November 30, 2010 | Sheet 12 of 46



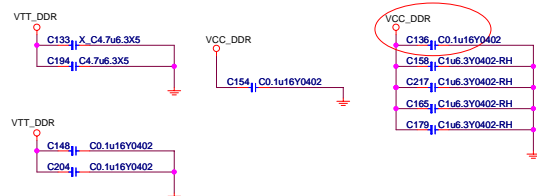
8	7	
DDRIII DIMM1_Channel A		



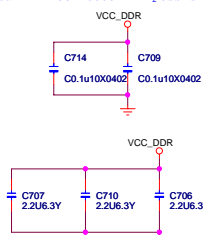
DIMM1 (CHANNEL-A)
ADDRESS = 0:0 [SA1:SA0]



CHANNEL A V SM VTT DECOUPLING CAPS



Layout note: Place capacitors between and near DDR connector if possible.



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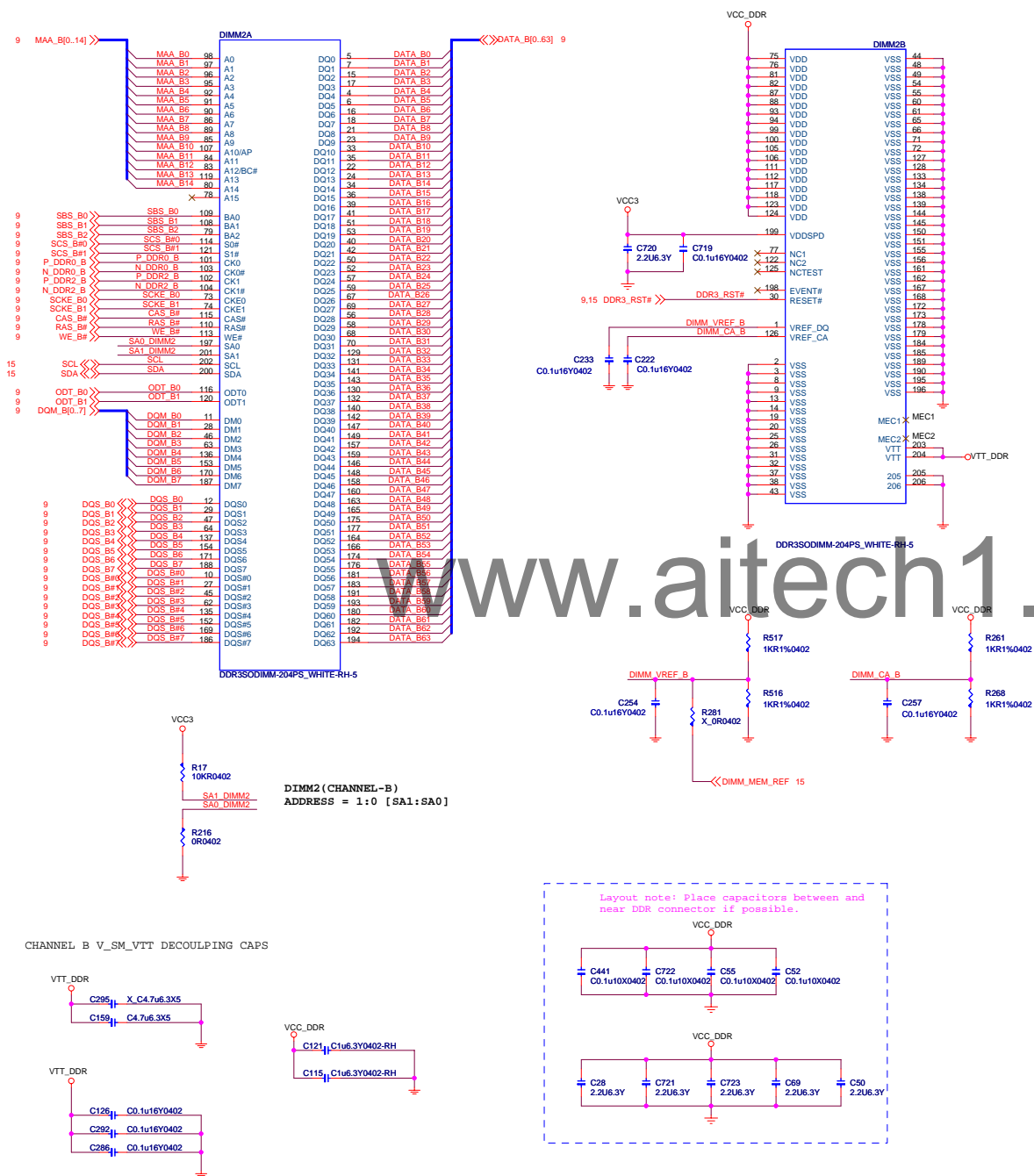
MS-AA51

Size	Document Description
Custom	DDR II DIMM A

Rev	1.01
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DDRIII DIMM2_Channel B	
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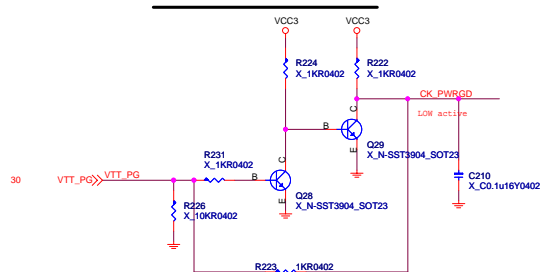
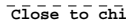


MICRO-STAR INT'L CO.,LTD

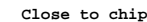
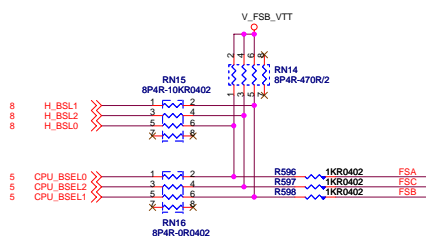
MS-AA51

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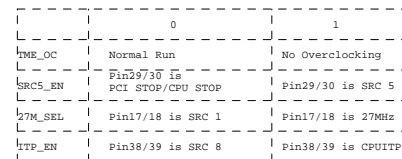
Rev	1.01
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BSEL[0..2] Level Shift



STRAPPING RESISTOR

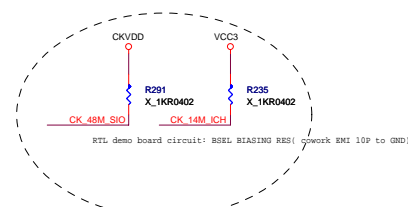


	0	1
IME_OC	Normal Run	No Overclocking
SRC5_EN	Pin29/30 is PCI STOP/CPU STOP	Pin29/30 is SRC 5
27M_SEL	Pin17/18 is SRC 1	Pin17/18 is 27MHz
1TP_EN	Pin38/39 is SRC 8	Pin38/39 is CPU1TP

CPU Frequency Selection

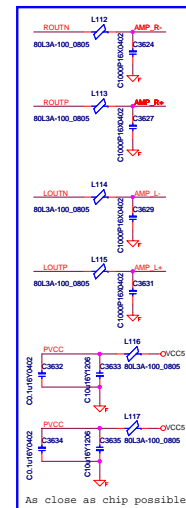
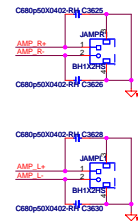
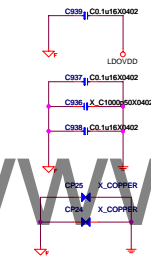
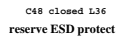
FS_C	FS_B	FS_A	CPU
0	0	1	133M
0	1	0	200M
0	0	0	266M
1	0	0	333M
1	1	0	400M

Only the selection in the table is valid



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Size Custom	Document Description CLK-RTM 875T-605	Rev 1.0
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The diagram shows the CMC-L12-1017014-RH connector with two views: a top view and a bottom view. The top view shows pins 1 through 8, with pins 1-4 labeled MD0+ and MD0-, and pins 5-8 labeled TR D0+ and TR D0-. The bottom view shows pins 1 through 8, with pins 1-4 labeled TR D2+ and TR D2-, and pins 5-8 labeled TR D3+ and TR D3-. The connector is labeled CMC-L12-1017014-RH.

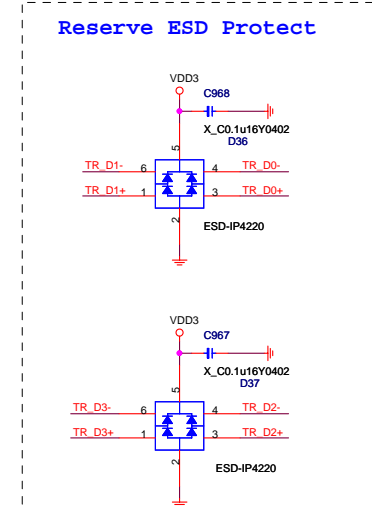
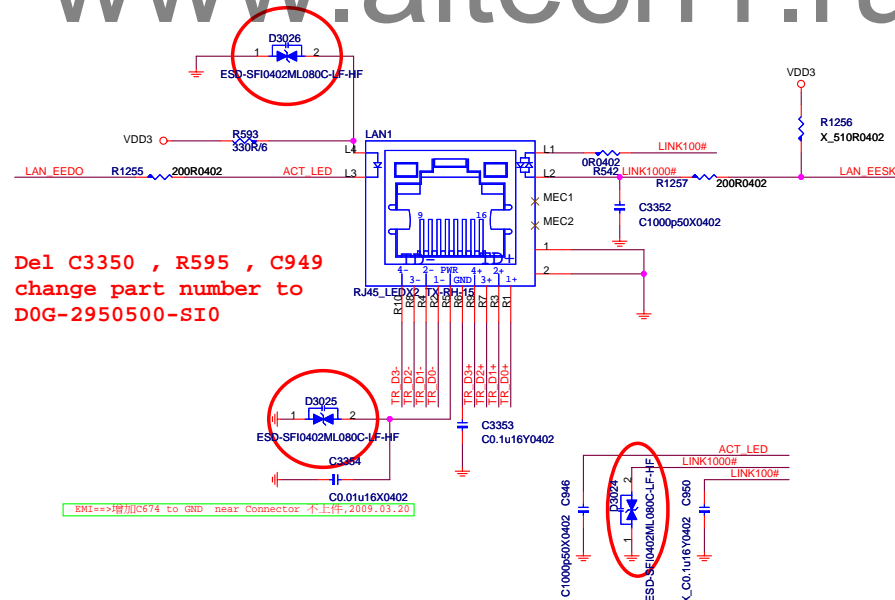
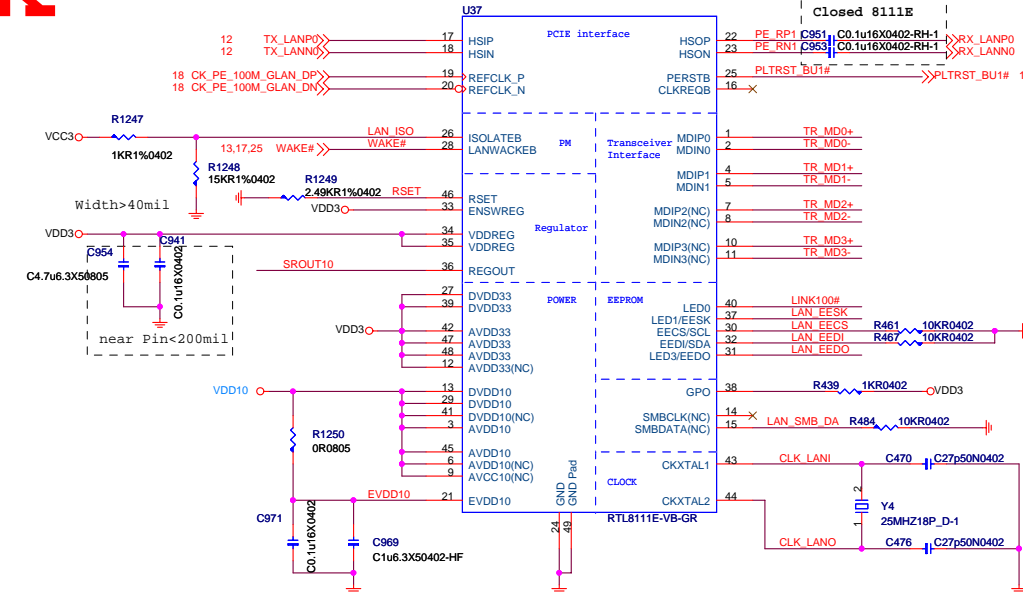
Pin	Signal
1	TR MD0+
2	TR MD0+
3	TR MD0+
4	TR MD0+
5	TR D0+
6	TR D0+
7	TR D0+
8	TR D0+




CMC-L12-1017014-RH

Pin	Signal
1	TR D2+
2	TR D2+
3	TR D2+
4	TR D2+
5	TR D3+
6	TR D3+
7	TR D3+
8	TR D3+

CMC-L12-1017014-RH

Del C3350 , R595 , C949
change part number to
D0G-2950500-SI0



<p>Giga-Lan</p>	
<p>Link Yellow Active Blinking 1000 Orange 100 Green 10 None</p>	
<p>L4 — </p>	
<p>L3 — Yellow</p>	
<p>Orange</p>	
<p>L2 —  </p>	
<p>L1 — Green</p>	



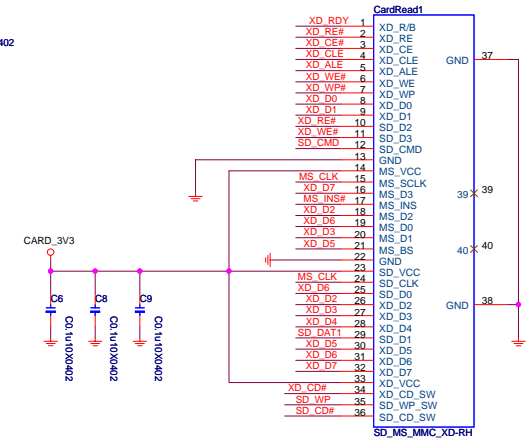
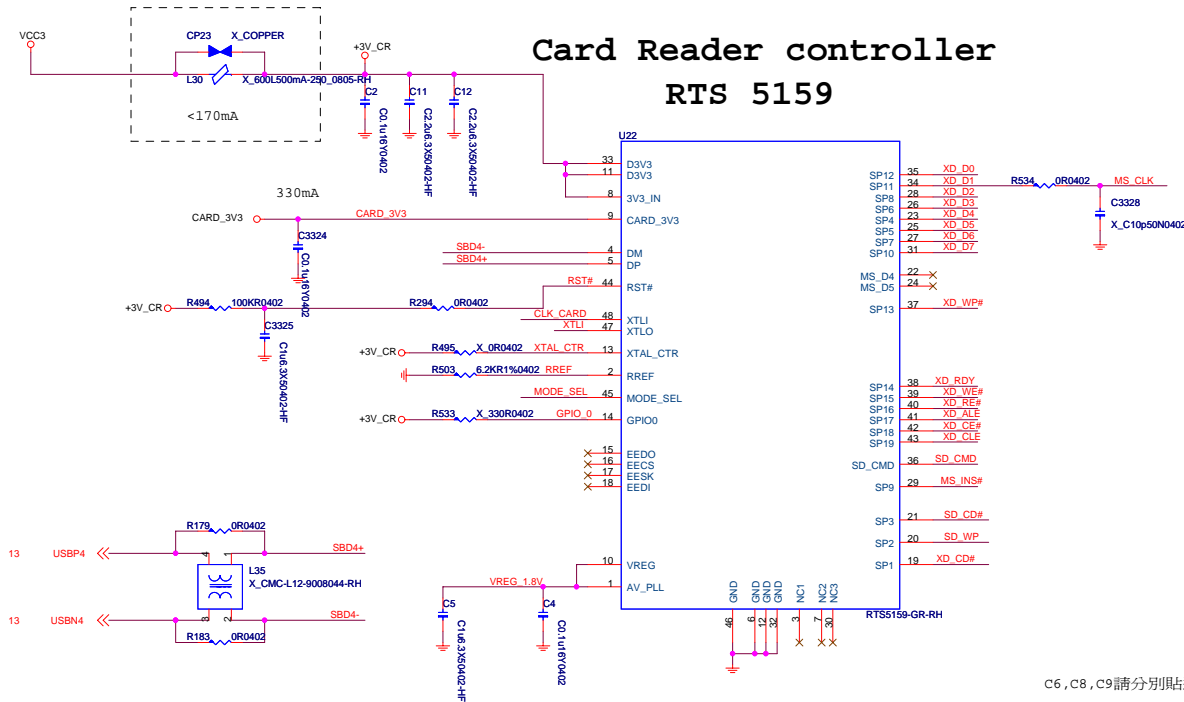
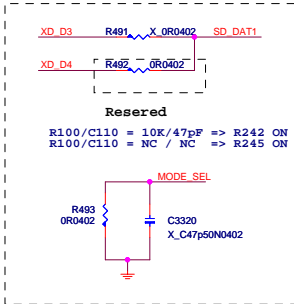
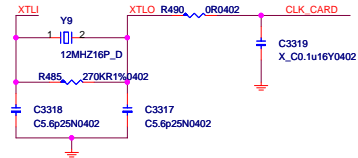
Size Custom	Document Description RTL8111E	Rev 1.01
Date: Tuesday, November 30, 2010		Sheet 20 of 46

ok

Card Reader controller RTS 5159

Flash Card Socket

XTAL_CTR:
Stuff R=48MHz CLK
Unstuff R=12MHz Crystal



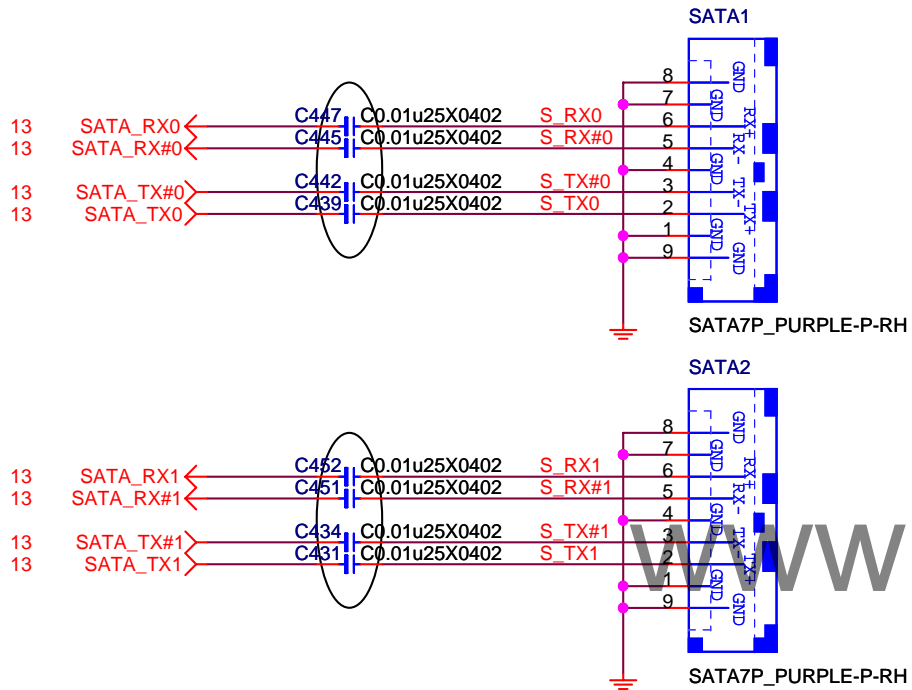
C6,C8,C9請分別貼近connector pin 14, pin23, pin33擺放

www.aitech1.ru

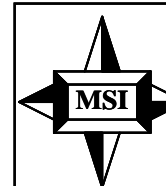
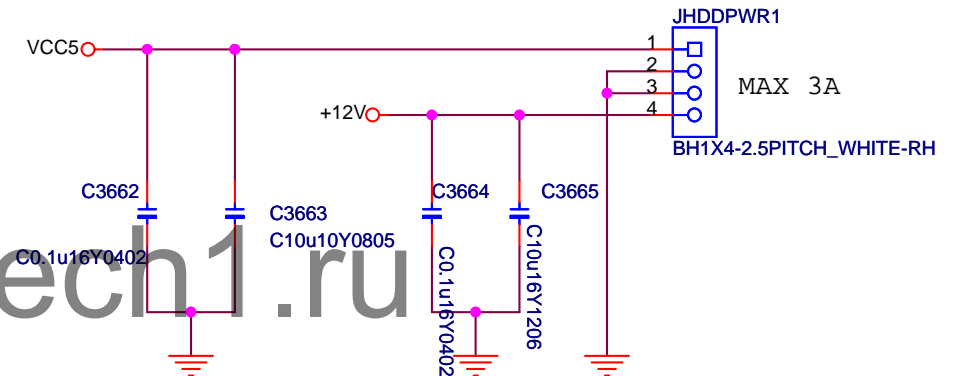
Title		
RTS5159		
Size	Document Number	Rev
CustomMS-AA51		1.01
Date:	Tuesday, November 30, 2010	Sheet 21 of 46

SERIAL ATA CONNECTOR BLOCK

ok



SATA Power



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MS-AA51

Size
A

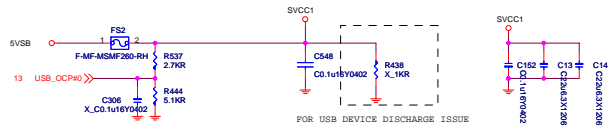
Document Description
SATA Connectors

Rev
1.01

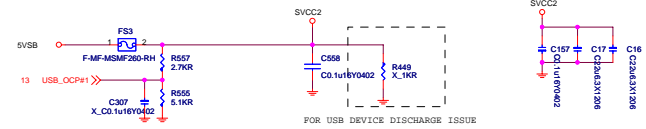
Date: Tuesday, November 30, 2010

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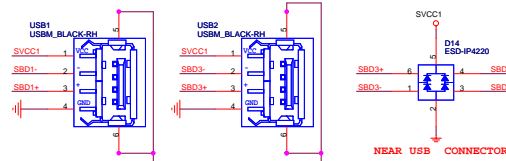
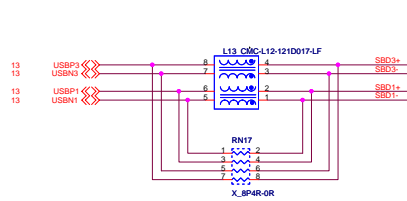
POWER CIRCUIT FOR USB PORT 1,3 (REAR)



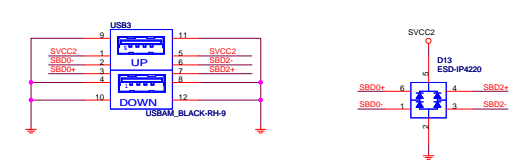
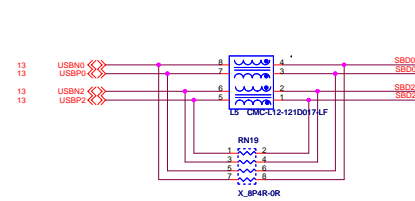
POWER CIRCUIT FOR USB PORT 0,2 (REAR)



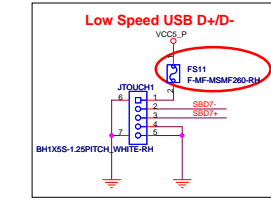
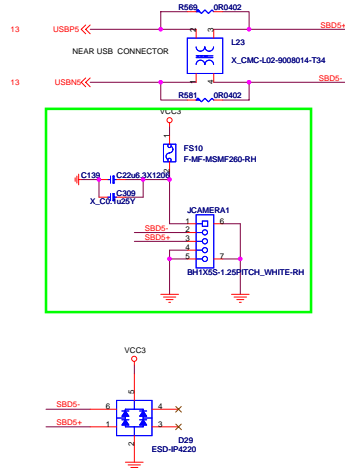
REAR USB CONNECTOR



SIDE USB CONNECTOR



REAR PANEL USB CONNECTOR FOR USB PORT 6,7



Video Connector

VGA線路上件

PLACE CLOSE TO VGA CONNECTOR

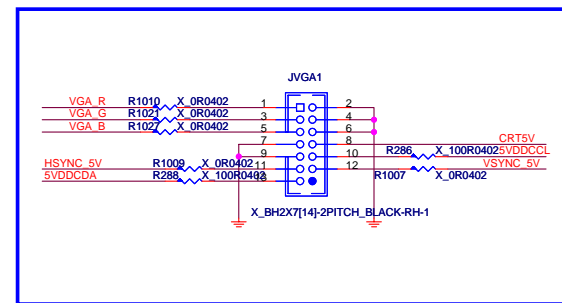
Thw R, G, B route lengths should be length match to 700mils.

as close as possible to VGA connector within 500Mil

www.aitech1.ru

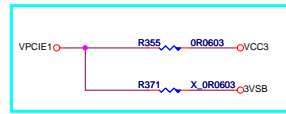
32 VGA_B << VGA_B
32 VGA_G << VGA_G
32 VGA_R << VGA_R

N51-15F0391-F02



MICRO-STAR INT'L CO.,LTD		
MS-AA51		
Size	Document Description	Rev
Custom	VGA Connector	1.01
Date:	Tuesday, November 30, 2010	Sheet 24 of 46

ok



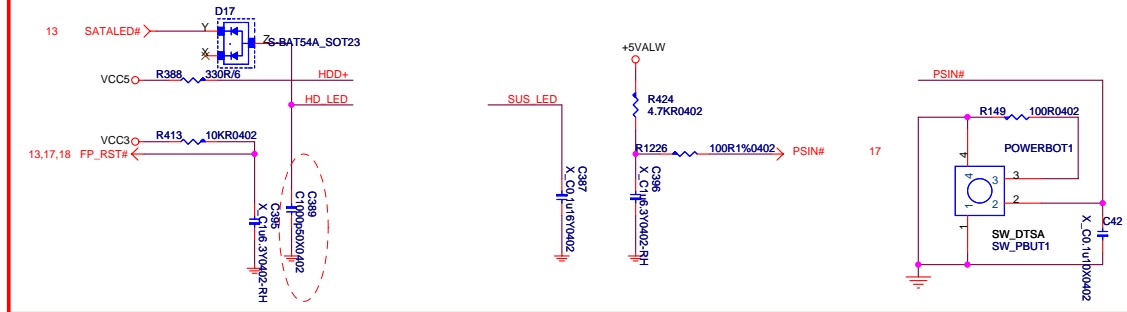
The diagram shows a blue rectangular box labeled "H1" at the top. Inside the box, the words "Spacer" and "Support" are stacked vertically. Below the box, a red vertical line extends downwards, ending in a red horizontal base. To the right of the red line, the text "E2B-1034010-RH" is written.

The schematic diagram illustrates the USB to RS-485 interface circuit. It features two USB pins, USBN6 and USBP6, connected to an RS-485 transceiver (L24, X_CMC-L1-92008044-R). The transceiver is connected to RS-485 lines SBD6- and SBD6+ through resistors R592, R591, and R0R402.



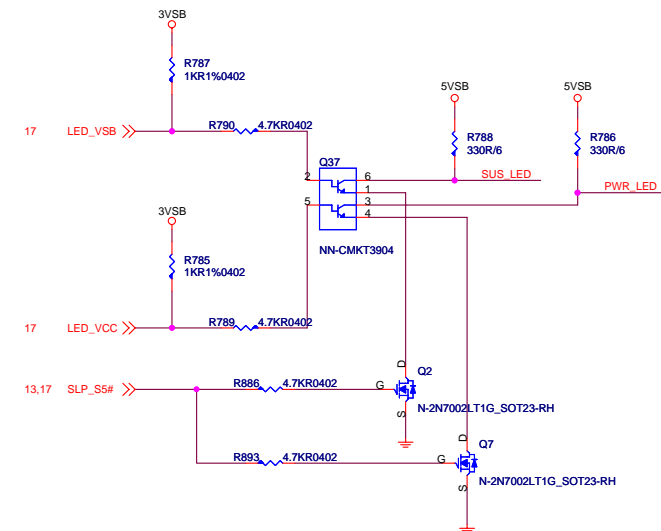
Rev	1.01
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INTEL/PB Front Panel Connector

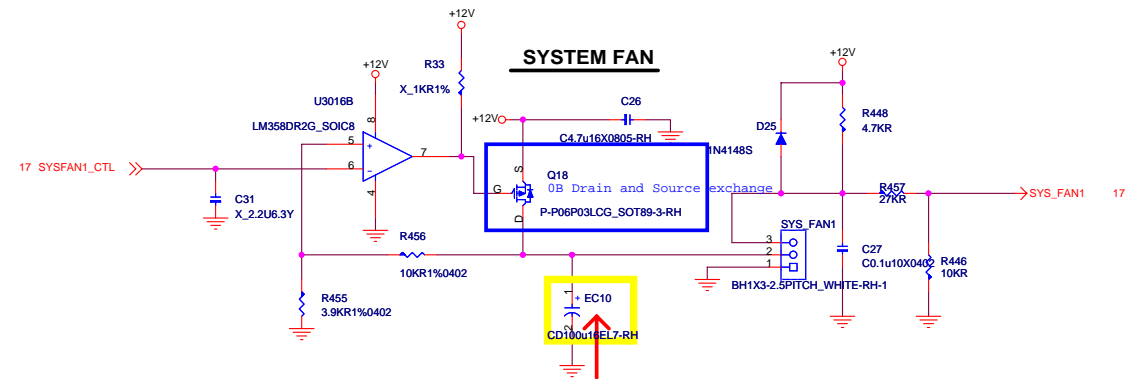
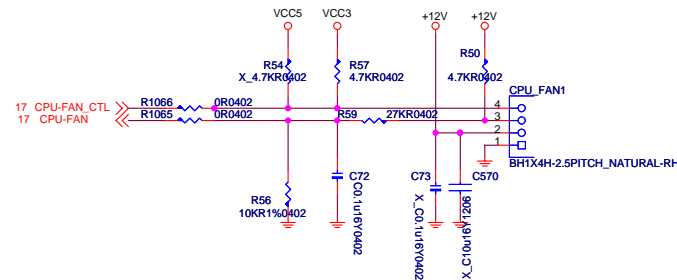


to change part number to D0C-010A701-K09

LED (for Fintek)



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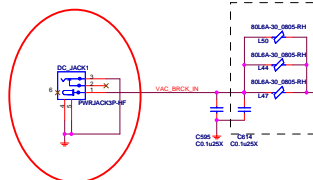
FAN控制線路的output電容改成DIP的100u



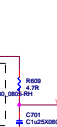
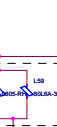
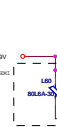
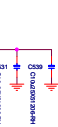
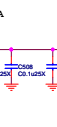
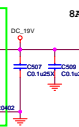
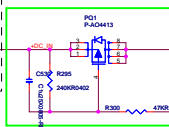
MICRO-STAR INT'L CO.,LTD

MS-AA51

Size	Document Description	Rev
Custom	Front Panel & FAN	1.01
Date:	Tuesday, November 30, 2010	Sheet 26 of 46

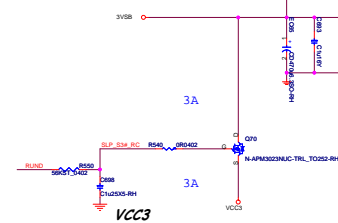


DC Voltage IN

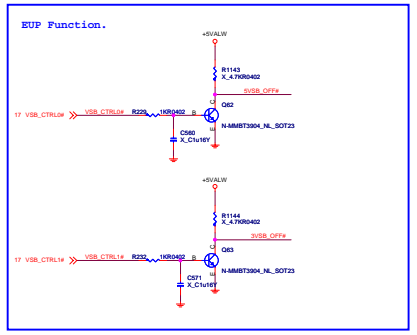
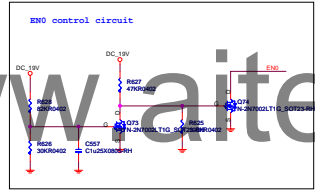


Place these CAPs close to FETs

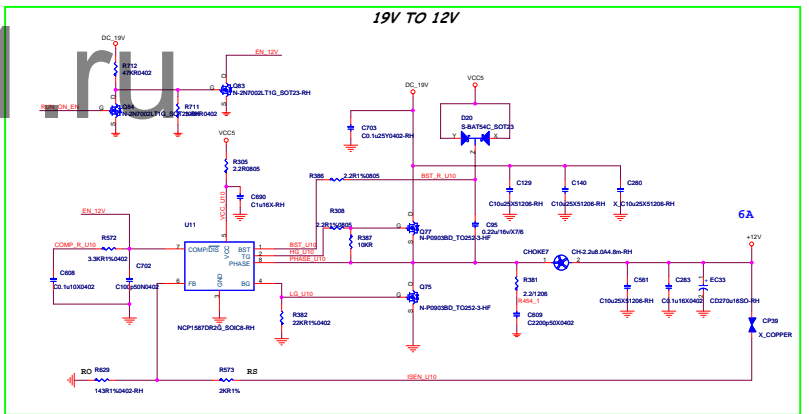
3VSB



EN0 open: LDO on and turn on switcher channel



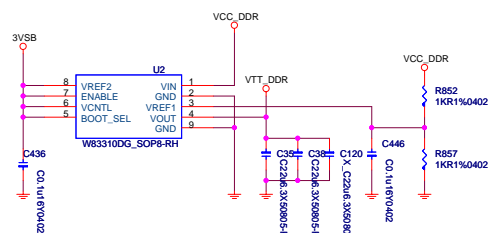
19V TO 12V



DC19V & SYSTEM & +12V POWER			
Rev	1	Sheet Number	1
Doc	DC19V-001	Doc Number	1
Date	10/01/2010	Date	10/01/2010

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

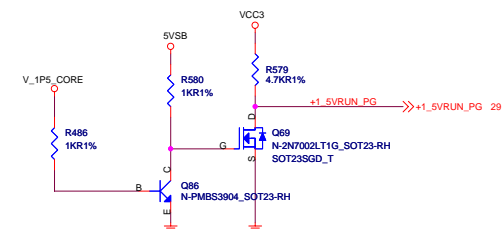
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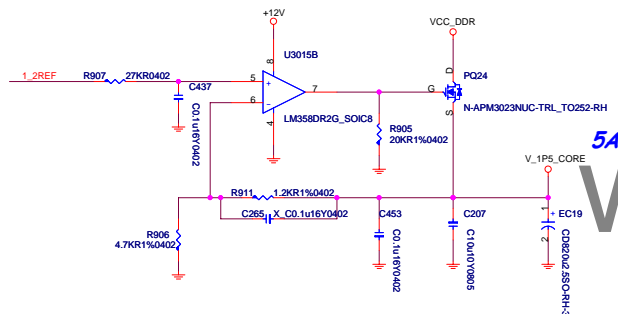
VTT_DDR 1.2A

ok

ok

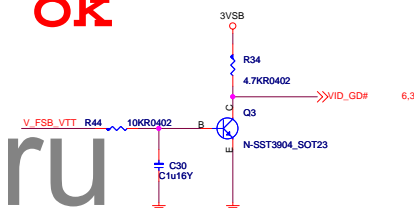


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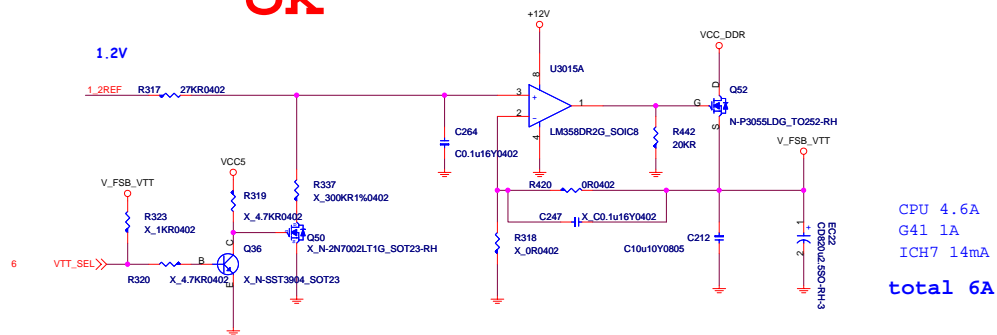
ok

ok



ok

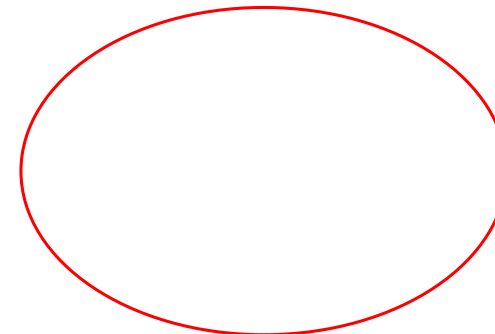
1.2V



```
CPU 4.6A
G41 1A
ICH7 14mA
total 6A
```

ok

Del CHIP_PWGD control circuit



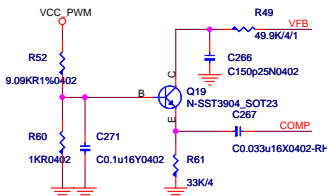
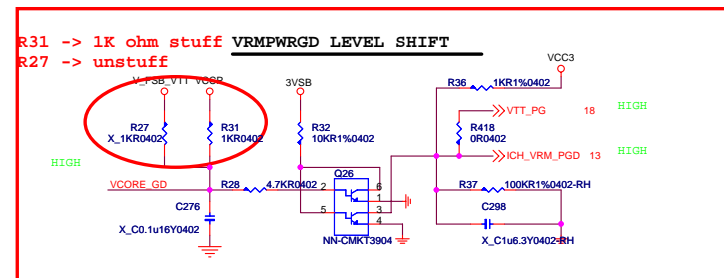
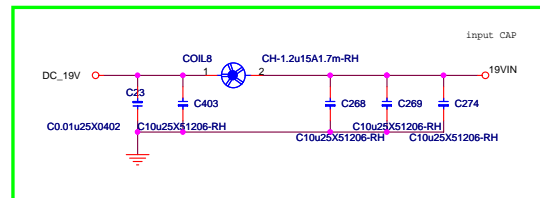
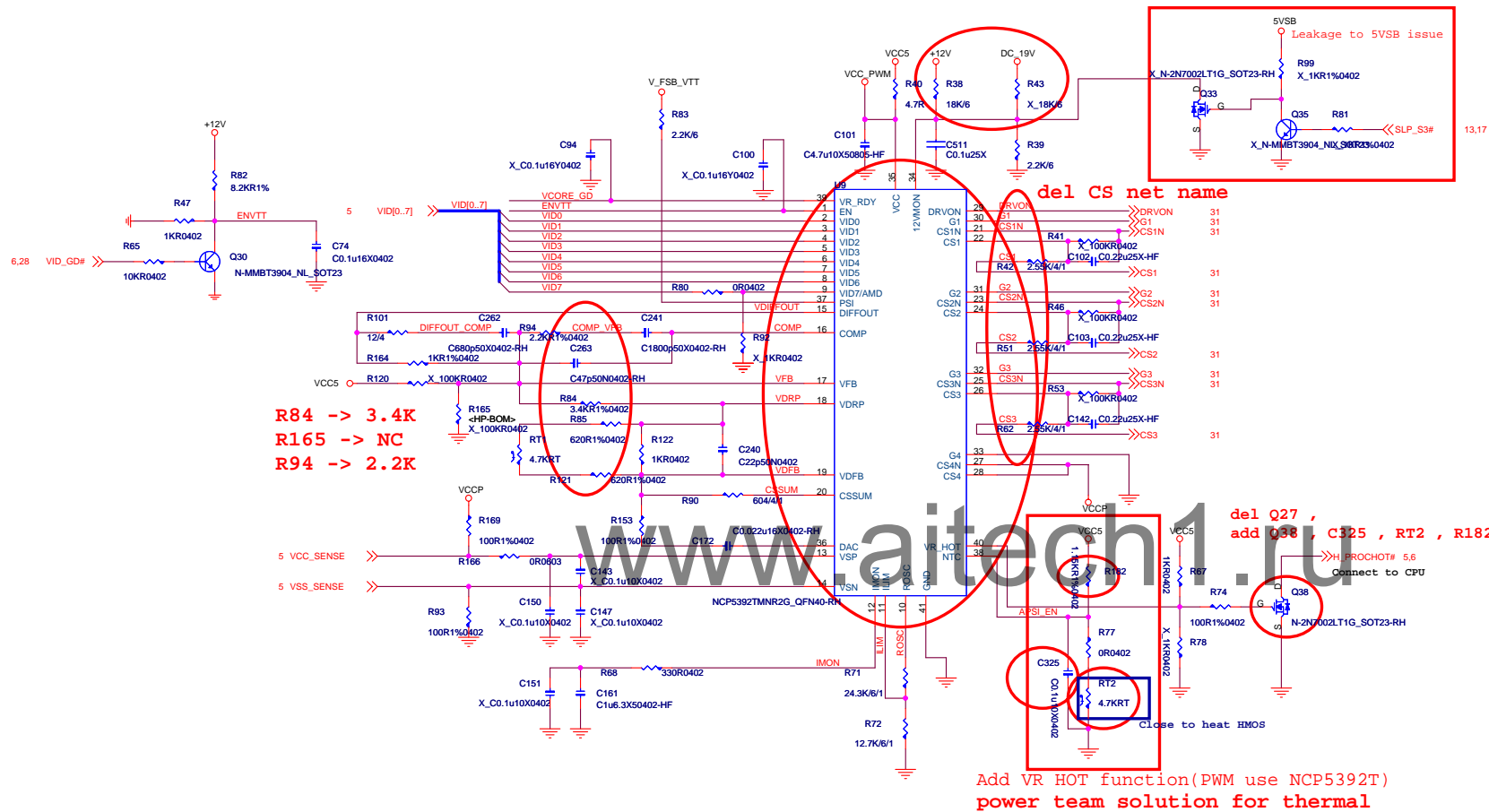
VTT_SEL	
0	VTT=1.1V for future CPU
1	VTT=1.2V for old CPU



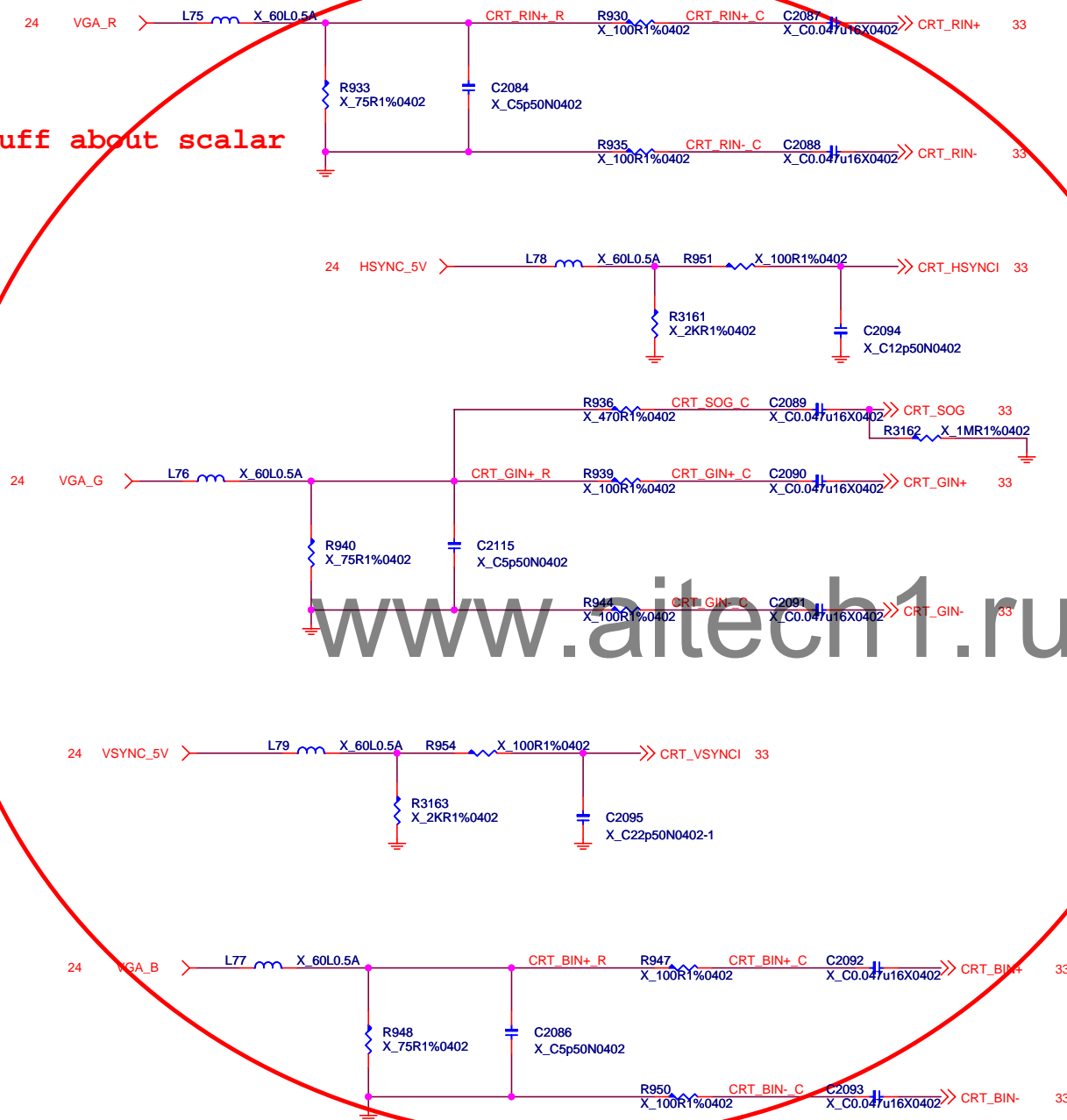
MS-AA51

Size Custom	Document Description ACPI controller	Rev 1.01
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To avoid VCCP leak voltage



circuit unstuff about scalar

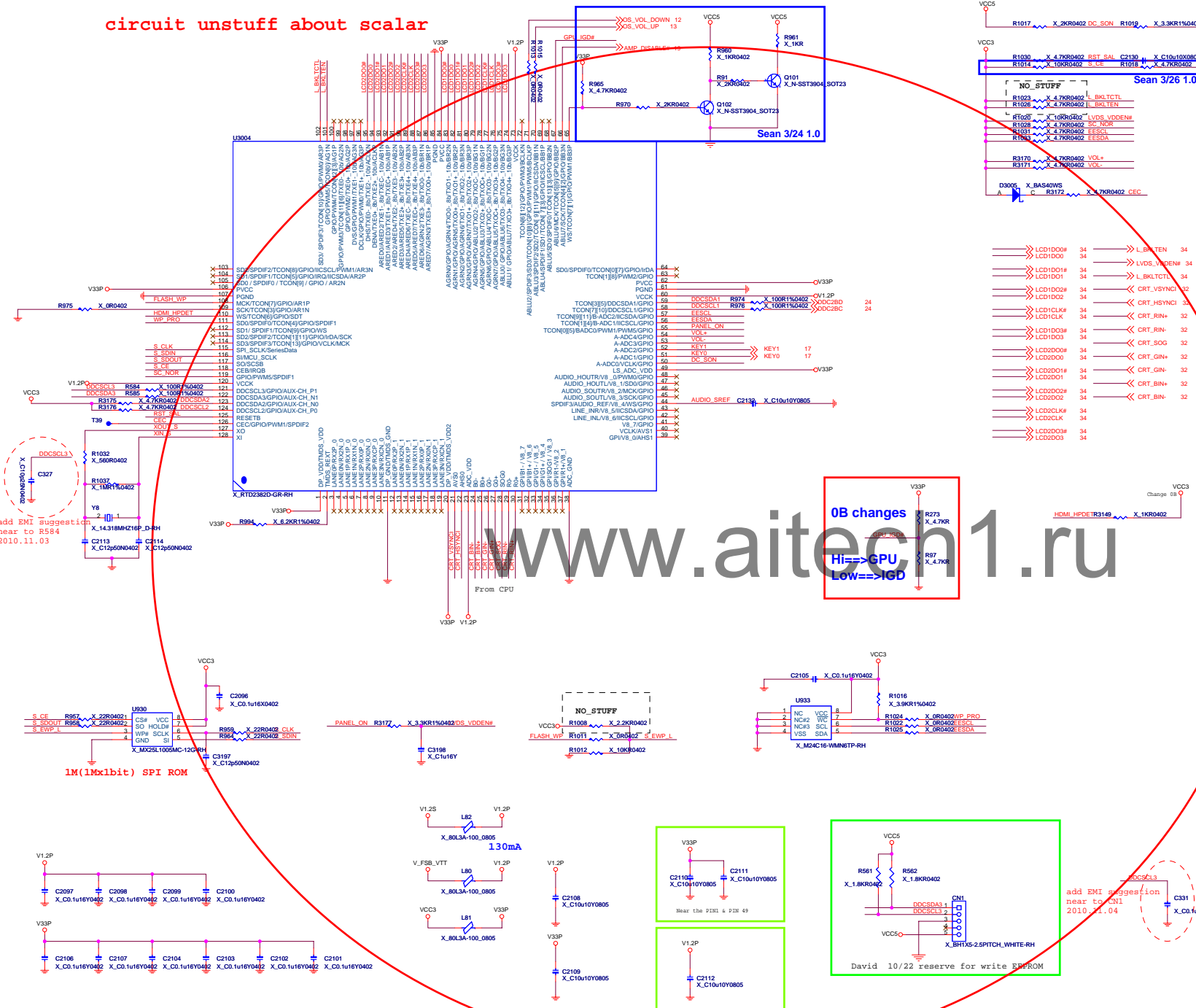


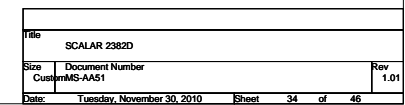
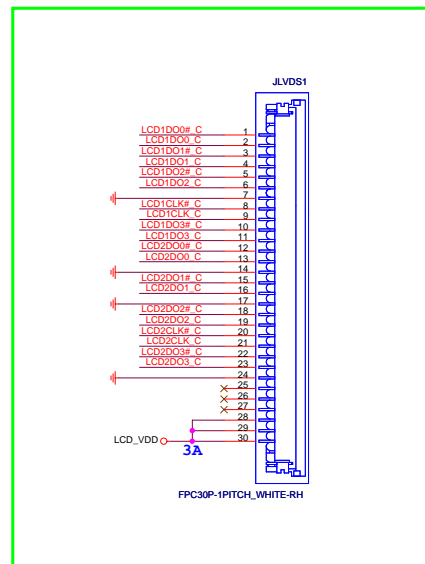
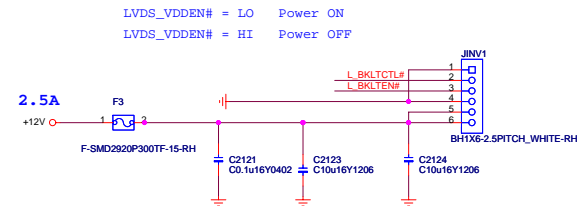
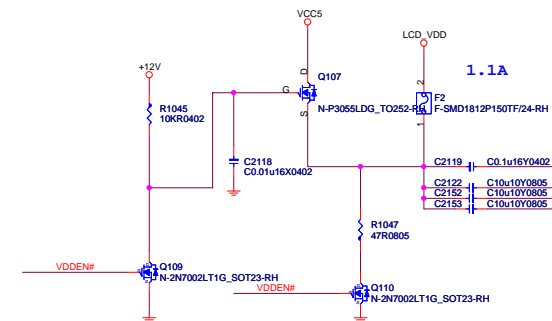
MICRO-STAR INT'L CO.,LTD

MS-AA51

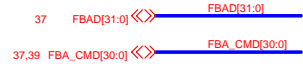
Size Custom	Document Description SCALAR 2382D	Rev 1.01
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circuit unstuff about scalar

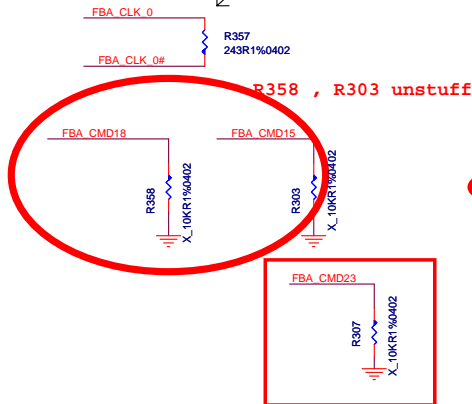




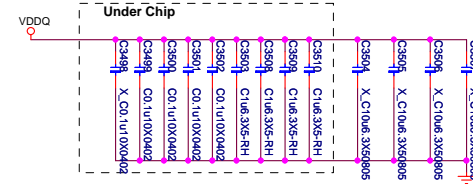
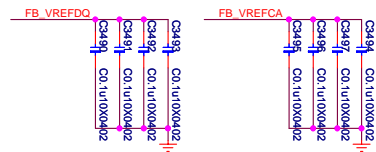
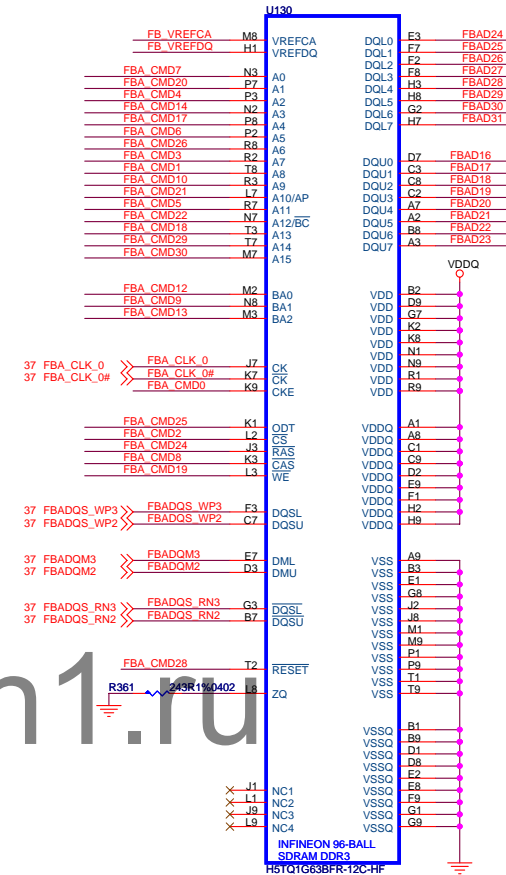
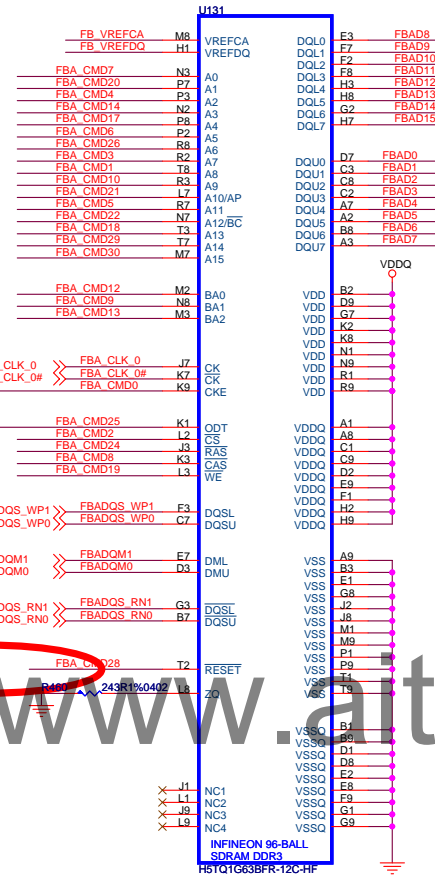
DDR3 64Mx16bits



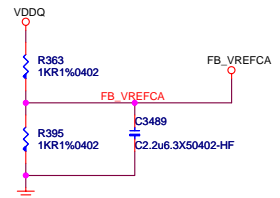
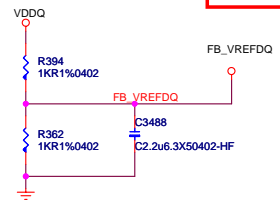
R357 need change to 242 ohm.



Del R377



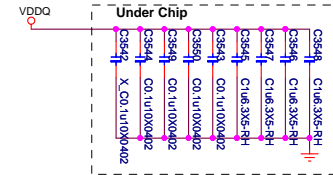
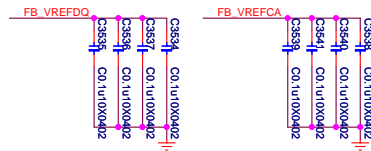
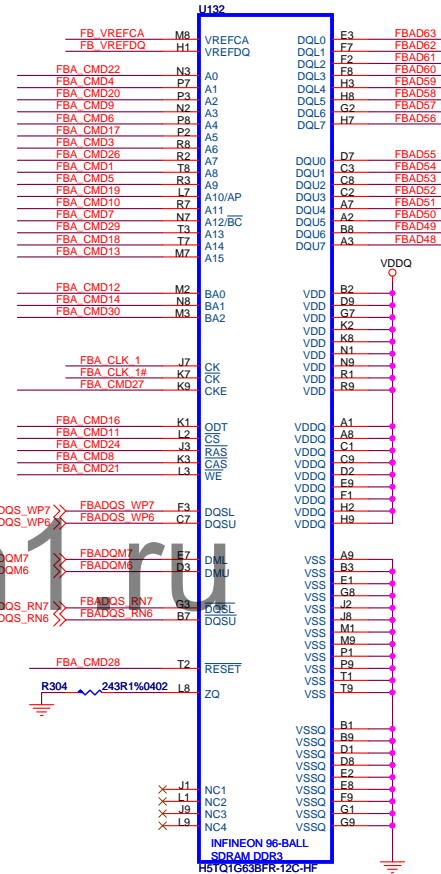
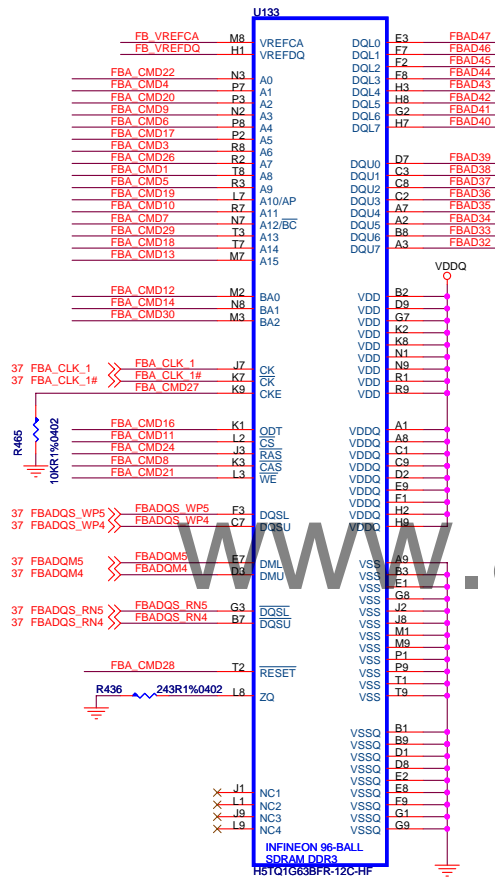
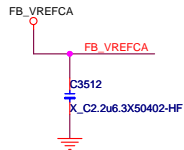
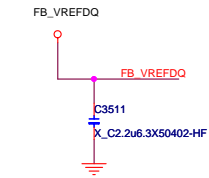
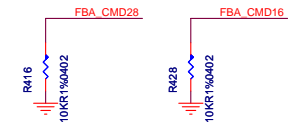
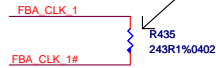
Each group(top & bottom) put a 0.1uF



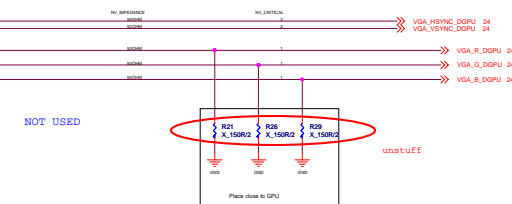
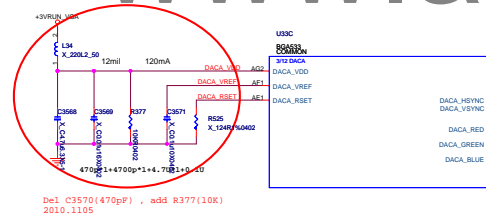
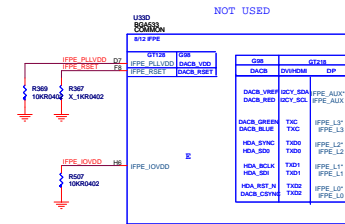
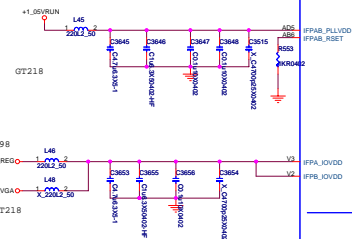
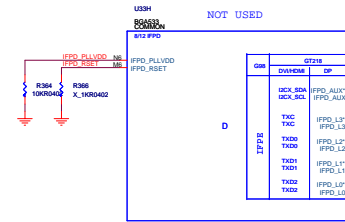
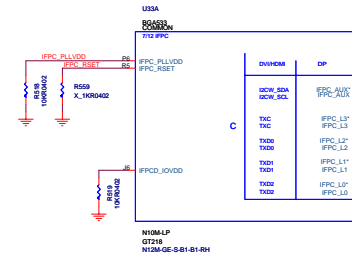
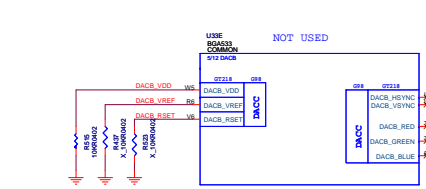
DDR3 64Mx16bits

CS# 29; 8
A2 22; 4
A3 24; 6
A4 0; 5
A5 2; 13
CKE 18; 7
ODT 30; 28

R264 need change to 242 ohm.1203

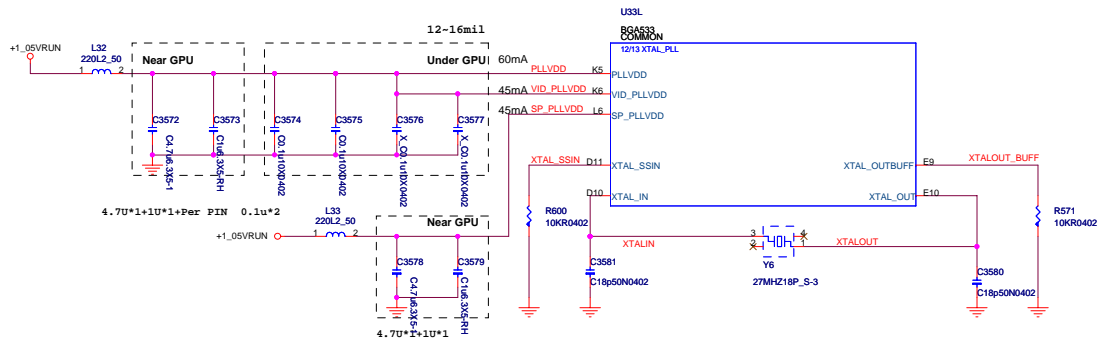


Each group(top & bottom) put a 0.1uF



US3J	US3J	US3J
AC11	AC11	AC11
AC12	AC12	AC12
AC13	AC13	AC13
AC14	AC14	AC14
AC15	AC15	AC15
AC16	AC16	AC16
AC17	AC17	AC17
AC18	AC18	AC18
AC19	AC19	AC19
AC20	AC20	AC20
AC21	AC21	AC21
AC22	AC22	AC22
AC23	AC23	AC23
AC24	AC24	AC24
AC25	AC25	AC25
AC26	AC26	AC26
AC27	AC27	AC27
AC28	AC28	AC28
AC29	AC29	AC29
AC30	AC30	AC30
AC31	AC31	AC31
AC32	AC32	AC32
AC33	AC33	AC33
AC34	AC34	AC34
AC35	AC35	AC35
AC36	AC36	AC36
AC37	AC37	AC37
AC38	AC38	AC38
AC39	AC39	AC39
AC40	AC40	AC40
AC41	AC41	AC41
AC42	AC42	AC42
AC43	AC43	AC43
AC44	AC44	AC44
AC45	AC45	AC45
AC46	AC46	AC46
AC47	AC47	AC47
AC48	AC48	AC48
AC49	AC49	AC49
AC50	AC50	AC50
AC51	AC51	AC51
AC52	AC52	AC52
AC53	AC53	AC53
AC54	AC54	AC54
AC55	AC55	AC55
AC56	AC56	AC56
AC57	AC57	AC57
AC58	AC58	AC58
AC59	AC59	AC59
AC60	AC60	AC60
AC61	AC61	AC61
AC62	AC62	AC62
AC63	AC63	AC63
AC64	AC64	AC64
AC65	AC65	AC65
AC66	AC66	AC66
AC67	AC67	AC67
AC68	AC68	AC68
AC69	AC69	AC69
AC70	AC70	AC70
AC71	AC71	AC71
AC72	AC72	AC72
AC73	AC73	AC73
AC74	AC74	AC74
AC75	AC75	AC75
AC76	AC76	AC76
AC77	AC77	AC77
AC78	AC78	AC78
AC79	AC79	AC79
AC80	AC80	AC80
AC81	AC81	AC81
AC82	AC82	AC82
AC83	AC83	AC83
AC84	AC84	AC84
AC85	AC85	AC85
AC86	AC86	AC86
AC87	AC87	AC87
AC88	AC88	AC88
AC89	AC89	AC89
AC90	AC90	AC90
AC91	AC91	AC91
AC92	AC92	AC92
AC93	AC93	AC93
AC94	AC94	AC94
AC95	AC95	AC95
AC96	AC96	AC96
AC97	AC97	AC97
AC98	AC98	AC98
AC99	AC99	AC99
AC100	AC100	AC100

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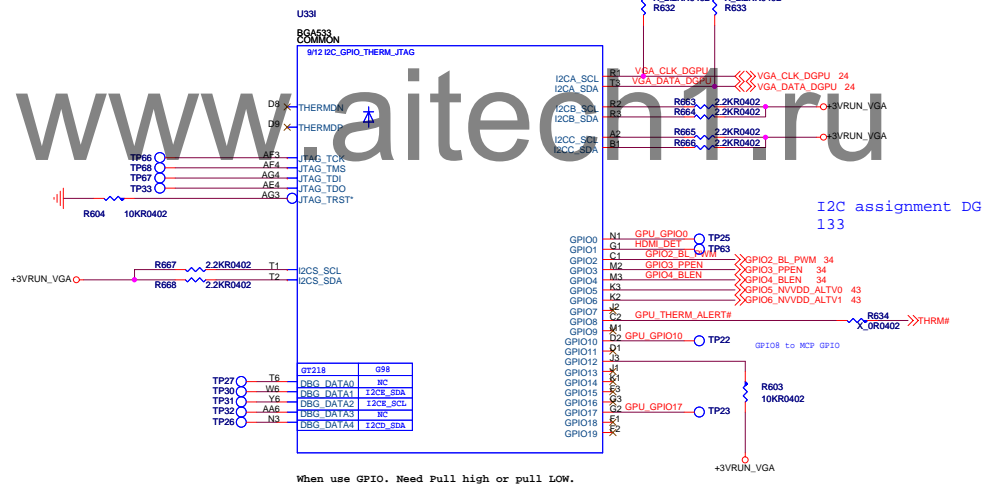


- * Near GPU : The total trace length measured from GPU ball to capacitor is no more than 150 mil
- * Under GPU : The total trace length measured from GPU ball to capacitor is no more than 750 mil

OPTIMUS MOT USED I2CB/I2CC, I2CA for debugging.1203

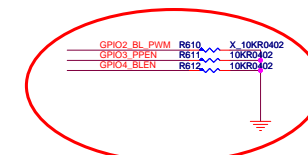
CRT

CRT

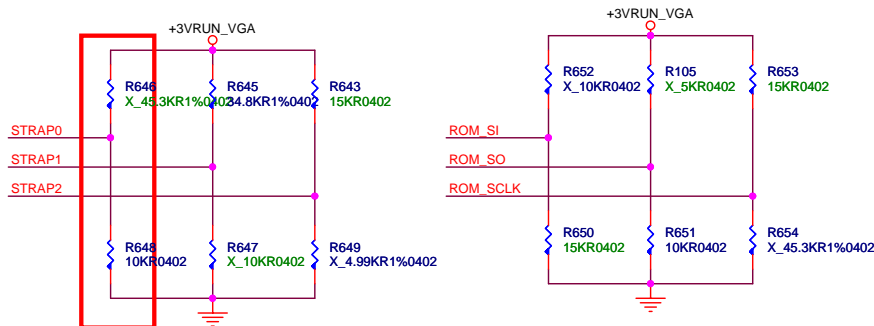
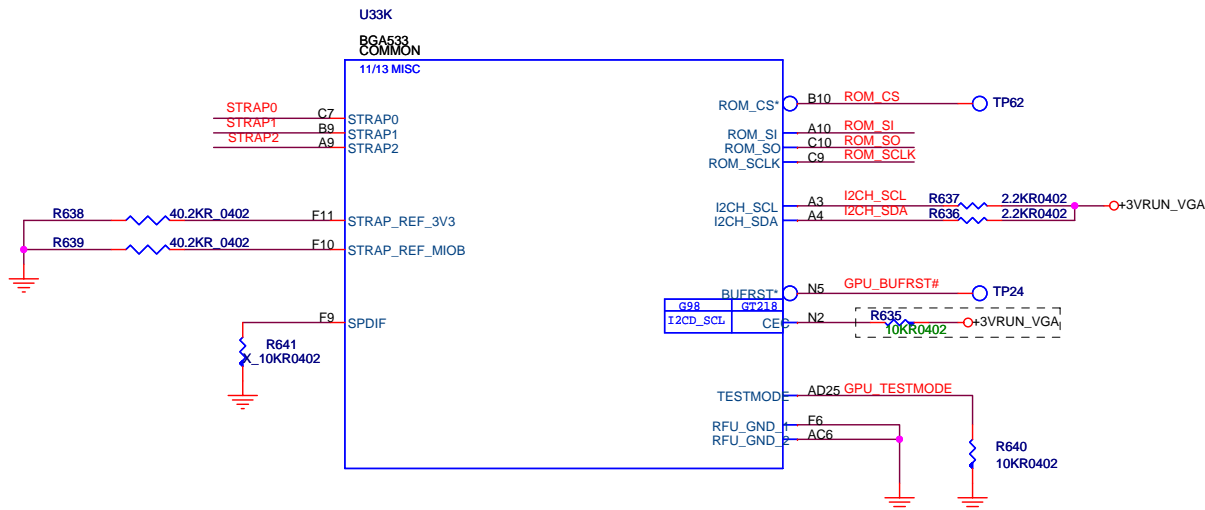


GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	
1	IN	N/A	DVI/HDMI LINKC HOTPLUG DETECT
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	HIGH	NVDD ALT0
6	OUT	HIGH	NVDD ALT1
7	OUT	HIGH	FBVDD VDD0
8	IN	LOW	OVERTEMP ALERT
9	OUT	LOW	THERMAL ALERT
10	OUT	HIGH	DYNAMIC FB VREF GDDR3 (not used for DDR2)
11	OUT	HIGH	SLI SYNC0 (not used for GB1-64)
12	IN	N/A	AC DETECT
13	OUT	LOW	POWER SUPPLY CONTROL0
14	OUT	HIGH	POWER SUPPLY CONTROL1
15	IN	N/A	HPD_E
16	IN	N/A	DVI_E
17	IN	N/A	HDMI_E
18	IN	N/A	DVI_F (not used)
19	IN	N/A	HDMI_F (not used)

GPIO6	GPIO5	NVDD(N12M-GE)
1	1	1.0V
1	0	
0	0	0.85V
0	1	0.85V



Add GPU Back Light control pull down resistor, R611,R612 stuff.
2010.11.04



Panel Strap 0 ("0000"=> 5K PD) is "CMIMEI M20003"
 N10M SE1 strap 0 ("0001"=>10k PD) => is "CMIMEI M20001"

OK	STRAP0	USER 3	0
		USER 2	0
		USER 1	0
	PD 10K	USER 0	1
OK	STRAP1	3GIO_PADCFG 3	1
		3GIO_PADCFG 2	1
	PU 35K	3GIO_PADCFG 1	1
		3GIO_PADCFG 0	0
OK	STRAP2	PCI_DEVID3	1
		PCI_DEVID2	0
	PD 5K	PCI_DEVID1	1
		PCI_DEVID0	0
OK	ROM_SCLK	PCI DEVID 4	1
		SUBVENDOR	0
	PU 15K	SLOT_CLK	1
		PEX_PLL_EN	0
OK	ROM_SI	RAMCFG 3	0
		RAMCFG 2	0
	PD 15K	RAMCFG 1	1
		RAMCFG 0	0
OK	ROM_SO	XCLK_417	0
		FB_0_BAR_SIZE	0
	PU 10K	SMB_ALT_ADDR	0
		VGA_DEVICE	1

PUN-04992-001-V01
 NOTEBOOK 1110

0X0A7A 1010
 N12M-GE-S-B1

VBIOS is in system bios
 GPU and MCH do not share a common clock
 disable pci express PLL termination

Hynix : 0010

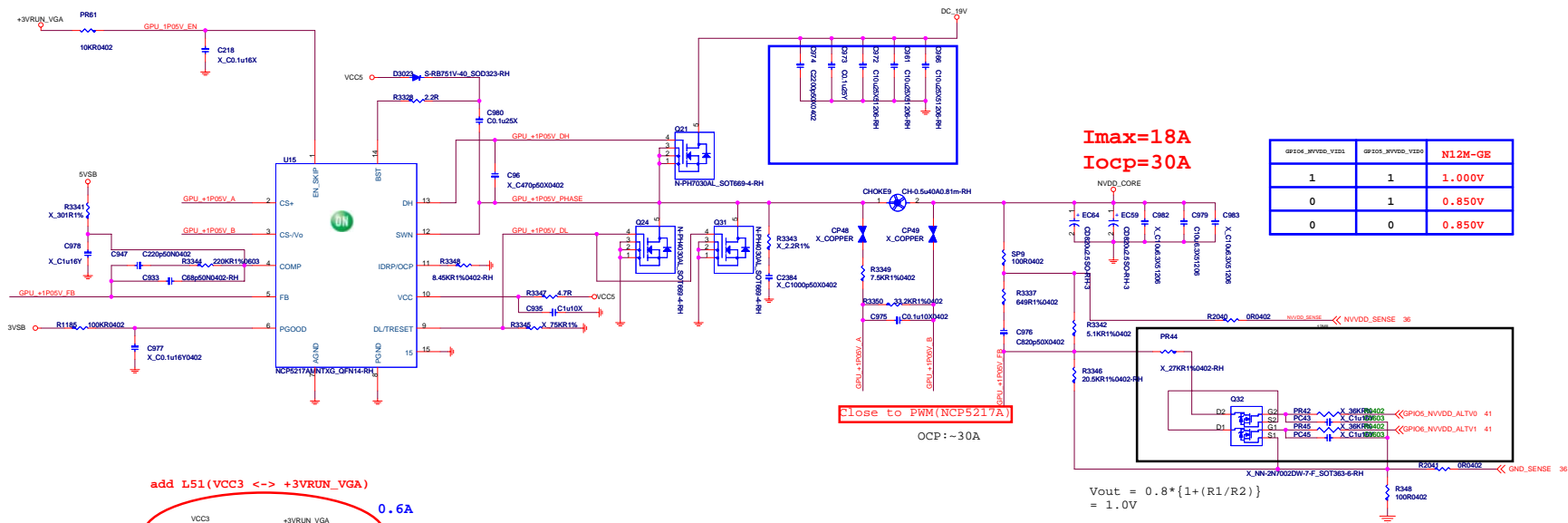
Have 27M hz CRYSTAL

SPEC have no TV function

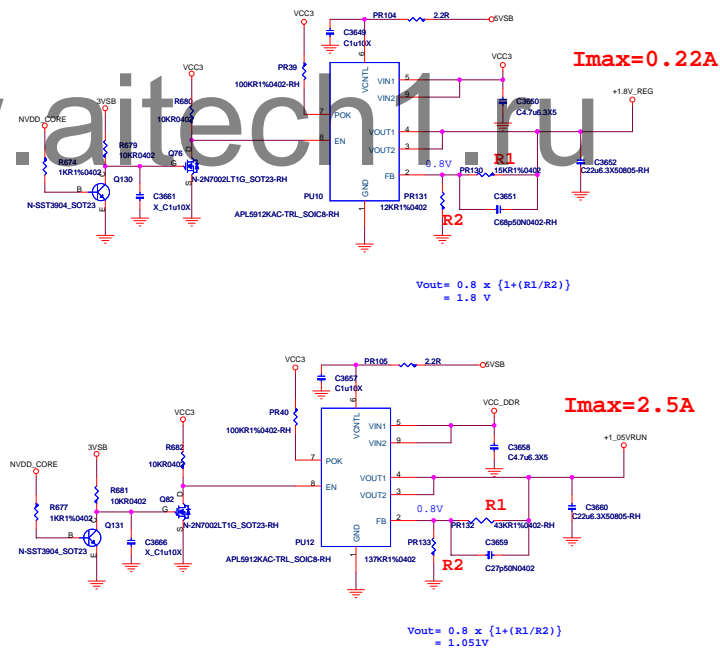
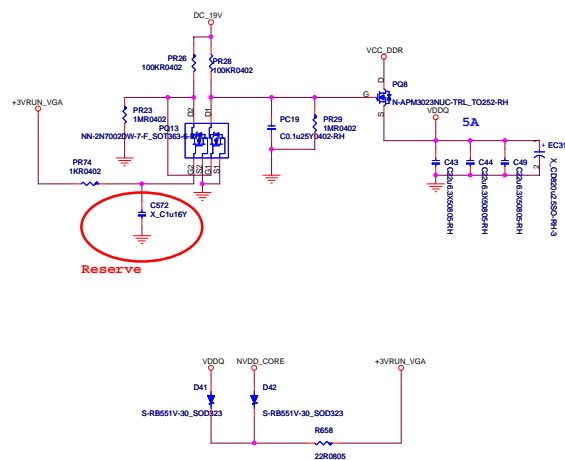
Rvalue	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

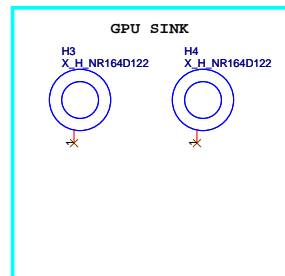
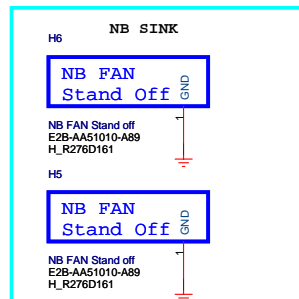
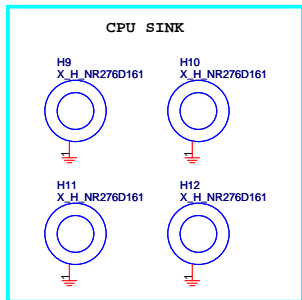
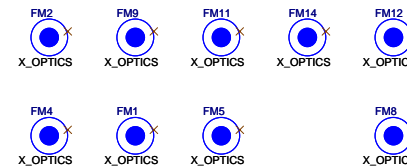
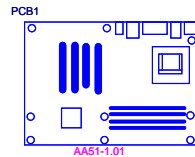
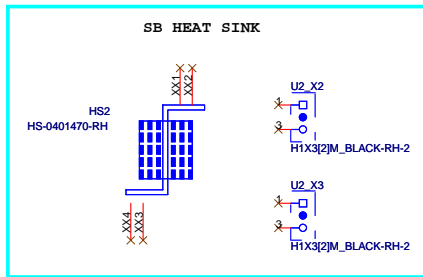
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GPU 1.05V Core Power

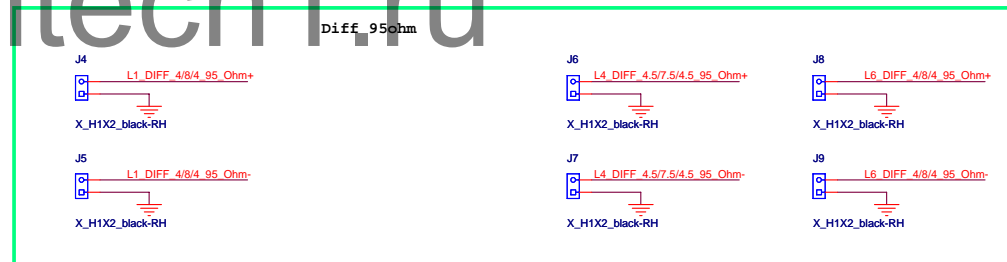
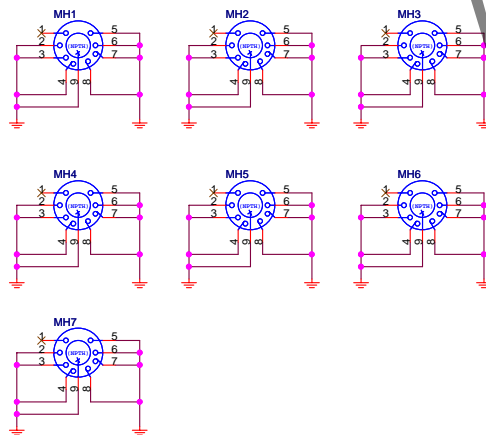
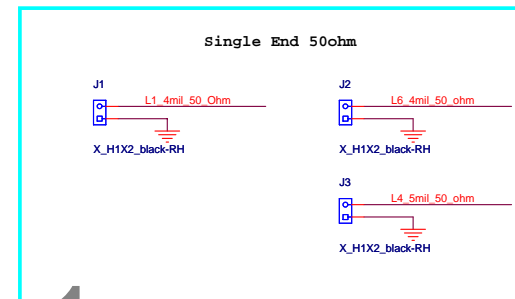


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Simulation



ICH7									
GPIO	Alt Func	PIN	I/O/NC	POWER	PU	SMI	TOL	DEFAULT	SIGNAL NAME
GPIO0	Unmultiplexed	AB18	I/O	CORE	N	Y	3.3V	GPI	GPIO(pull high)
GPIO1	REQ5#	C8	I/O	CORE	N	Y	5V	GPI	PREQ#5
GPIO2	PIRQE#	G8	I/OD	CORE	N	Y	5V	GPI	GPIO2(pull high)
GPIO3	PIRQF#	F7	I/OD	CORE	N	Y	5V	GPI	GPIO3(pull high)
GPIO4	PIRQG#	F8	I/OD	CORE	N	Y	5V	GPI	GPIO4(pull high)
GPIO5	PIRQH#	G7	I/OD	CORE	N	Y	5V	GPI	GPIO5(pull high)
GPIO6	Unmultiplexed	AC21	I/O	CORE	N	Y	3.3V	GPI	ATADET0
GPIO7	Unmultiplexed	AC18	I/O	CORE	N	Y	3.3V	GPI	STRAPPED HI
GPIO8	Unmultiplexed	E21	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO9	Unmultiplexed	E20	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO10	Unmultiplexed	A20	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO11	SMBALERT#	B23	I/O	Resume	N	Y	3.3V	Native	STRAPPED HI
GPIO12	Unmultiplexed	F19	I/O	Resume	N	Y	3.3V	GPI	SIO_PME#
GPIO13	Unmultiplexed	E19	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO14	Unmultiplexed	R4	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO15	Unmultiplexed	E22	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO16	Unmultiplexed	AC22	I/O	CORE	N	N	3.3V	GPO	NC
GPIO17	GNT5#	D8	I/O	CORE	N	N	3.3V	GPO	STRAPPED L
GPIO18	Unmultiplexed	AC20	I/O	CORE	N	N	3.3V	GPO	NC
GPIO19	SATA_1GP	AH18	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO20	Unmultiplexed	AF21	I/O	CORE	N	N	3.3V	GPO	NC
GPIO21	SATA_0GP	AF19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO22	REQ4#	A13	I/O	CORE	N	N	3.3V	Native	STRAPPED HI
GPIO23	LDRQ_1#	AA5	I/O	CORE	N	N	3.3V	Native	STRAPPED HI
GPIO24	Unmultiplexed	R3	I/O	Resume	N	N	3.3V	GPO	NC
GPIO25	Unmultiplexed	D20	I/O	Resume	Y	N	3.3V	GPO	GPIO25(high 7507,low 7398)
GPIO26	Unmultiplexed	A21	I/O	Resume	N	N	3.3V	GPO	USB_EN
GPIO27	Unmultiplexed	B21	I/O	Resume	N	N	3.3V	GPO	NC
GPIO28	Unmultiplexed	E23	I/O	Resume	N	N	3.3V	GPO	NC
GPIO29	OC5#	C3	I/O	Resume	N	N	3.3V	GPI	USB_OCP#2
GPIO30	OC6#	A2	I/O	Resume	N	N	3.3V	GPI	USB_OCP#3
GPIO31	OC7#	B3	I/O	Resume	N	N	3.3V	GPI	USB_OCP#3
GPIO32	Unmultiplexed	AG18	I/O	CORE	N	N	3.3V	GPO	BIOS_WP#(fill with 1)
GPIO33	Unmultiplexed	AC19	I/O	CORE	N	N	3.3V	GPO	NC
GPIO34	Unmultiplexed	U2	I/O	CORE	N	N	3.3V	GPO	NC
GPIO35	SATACLKREQ#	AD21	I/O	CORE	N	N	3.3V	GPO	NC
GPIO36	SATA2GP	AH19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO37	SATA3GP	AE19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO38	Unmultiplexed	AD20	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO39	Unmultiplexed	AE20	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO48	GNT4#	A14	I/O	CORE	N	N	3.3V	Native	STRAPPED HI
GPIO49	CPUPWRGD	AG24	I/O	V_CPU_IO	N	N	V_CPU_IO	Native	H_PWRGD

Following are the GPIOs that need to be terminated properly if not used:
GPIO[39:36,23:21,19,7:0]: default as inputs and should be pulled up to Vcc3_3 if unused.
GPIO[31:29,15:8]: default as inputs and should be pulled up to VccSus3_3 if unused.

SIO Fintek71882FG(CONTINUE)

GPIO	Alt Func	PIN	Usage	Input/Output	NOTES
GPIO0	VIDOUT0	49	MCH_BSEL0	O12	
GPIO1	VIDOUT1	50	MCH_BSEL1	O12	
GPIO2	VIDOUT2	51	MCH_BSEL2	O12	
GPIO3	VIDOUT3	52	NC	O12	
GPIO4	VIDOUT4	53	NC	O12	
GPIO5	VIDOUT5/SIC	54	NC	I/OD12t	
GPIO6	SLOT0CC#	55	GPO	I/OD12t	
GPIO7	Turbo1#/WDTRST#	56	WDTRST#	OD12-5v	
GPIO15	LED_VSB/ALERT#	64	LED_VSB	OD12	
GPIO16	LED_VCC/Turbo2#	65	LED_VCC	OD12	
GPIO20	PCIRST1#	74	PCIRST1#	OD12	
GPIO21	PCIRST2#	75	PCIRST2#	O12	
GPIO22	PCIRST3#	76	PCIRST3#	O12	
GPIO23	RSTCON#	77	RSTCON#	OD12	
GPIO24	ATXPG_IN	78	ATXPG_IN	AIN	
GPIO32	PWROK	84	PWROK	OD12	
GPIO26	PWSIN#	80	PWSIN#	INts5v	
GPIO27	PWSOUT#	80	PWSOUT#	OD12	
GPIO30	S3#	82	S3#	INts5v	
GPIO31	PSON#	83	PSON#	OD12-5v	
GPIO33	RSMRST#	85	RSMRST#	OD12	
GPIO40	FANIN3	25	FANIN3	INts5v	
GPIO41	FAN_CTL3	26	FAN_CTL3(NC)	OD12-5v	
GPIO25	PME#	79	PME#	OD12-5v	
GPIO10	SPI_SLK/FANIN4	59	GPIO10(NC)	I/OD12t	
GPIO11	SPI_CS0#/FANCTL4	60	GPIO11(NC)	I/OD12t	
GPIO12	SPI_MISO/FANCTL1_1	61	GPIO12(NC)	I/OD12t	
GPIO13	SPI_MOSI/BEEP	62	BEEP(NC)	OD24	
GPIO14	FWH_DIS/WDTRST#/SPI_CS1#	63	GPIO14	I/OD12t	
GPIO42	IRTX	27	IRTX	O12	
GPIO43	IRRX	28	IRRX	INts	
GPIO17		66	NC	I/OD12t	

PCI Config.

DEVICES	MCP1 INT	PIN REQ#/GNT#	IDSEL	CLOCK
PCI1	PIRQ#A PIRQ#B PIRQ#C PIRQ#D	PREQ#0 PGNT#0	AD16	PCI_CLK0
PCI2	PIRQ#B PIRQ#C PIRQ#D PIRQ#A	PREQ#1 PGNT#1	AD17	PCI_CLK1

DDRII DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM A	A0H	P_DDR0_A/N_DDR0_A P_DDR1_A/N_DDR1_A P_DDR2_A/N_DDR2_A
DIMM B	A4H	P_DDR0_B/N_DDR0_B P_DDR1_B/N_DDR1_B P_DDR2_B/N_DDR2_B

JUMPER SETTING

JBAT1	(1-2)NORMAL	(2-3)CLEAR
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Change History

Item	Description	Cause	Page	Ver
1	Copy from MS-7592-6.1 0607FINAL.DSN		A11	0A

Item	Cause	Description	Page	Ver
1	To correct CPU pull high/low resistor	RN6.6 -> GND RN6.8 -> VTT_OUT_RIGHT	5	1.0
2	Modify VBAT daul power from +3VALW/Battery	D30.X -> +3VALW	13	1.0
3	Volume function useless	Unstuff U56,U57,U924,VOL_UP1,VOL_DOWN2,R140,R141,R340,R376,R326,R342,C392,C394,C399,C400 Unstuff R849,R858	13 17	1.0
4	TPM function useless	Delete JTPM1,C93 R263,C226	17 18	1.0
5	Delete double pull high resistor	Delete R543,R599,R847	17	1.0
6	INTEL CPU setting(SIO)	R859 stuff	17	1.0
6	FAN control(SIO)	R844 unstuff	17	1.0
7	VGA function useless	VGA circuit unstuff R21,R26,R29 unstuff	24 40	1.0
8	To change part number	CPU1(Socket) -> N12-7750020-F02 HDDLED1,POWERLED1 -> DOC-010A701-K09 DC_JACK1 -> N92-03M0351-AF2 L122,L123 -> L12-1017014-N52	5,6,7 26 27 20	1.0
9	CHIP_PWGD controled from SIO directly	Delete D3031 Delete Q87,Q39,R296,R297,R301,R306	17 28	1.0
10	VCC_DDR voltage set to 1.55V	R1182 -> 8.06K ohm	29	1.0
11	VRM circuit modify	R84 -> 3.4K , R94 -> 2.2K , R165 -> unstuff Delete U9.22 , U9.24 , U9.26 net name(CS*)	29	1.0
12	Add VRM thermal protect circuit	Add Q38,R67,R74,R78,R182,RT2,C325	30	1.0
13	To avoid VCCP leak voltage	Add R38(18K ohm,stuff),Q33,Q35,R99,R81	30	1.0
14	To change VCORE_GD pull high from VCCP	R31 -> stuff , R27 -> unstuff	30	1.0
15	Scalar function useless	Scalar circuit unstuff	32,33	1.0
16	To correct back light up/down control	R676.2 -> Q43.D , R659 -> unstuff	34	1.0
17	To correct back light enable	GPIO4_BLEN -> L_BKLTEN#	34	1.0
18	Modify GPU DDR3 pull low resistor	R303,R358 -> unstuff Delete R377	38	1.0
19	Reserve VDDQ delay circuit	Add C572(unstuff)	43	1.0
20	To correct VCC3 -> +3VRUN_VGA directly	Delete PR70,PR71,PR66,PR73,PR72,PQ23,PQ25,PC20,C3594,C3595 Add L51	43	1.0
21	To improve DFM	Delete RN48,RN54 ; add R496,R498,R502,R506,R508,R509 Delete RN35,RN36,RN37,RN61 ; add R464,R466,R470,R471,R476,R487,R488,R489,R500,R501,R510,R511,R512	12 13	1.0
22	Add EMI suggestion and part stuff	Add C327,C328,C329,C330 C324,C323,C322,C314,C315,C316,C317,C321,C20,C21,C22,C310,C296,C294,C136,C290,C297,C304,C302,C2382,R1174,R545,R623, C23,C691,C695,C2383,R3330,C389,C214,C502,C917,C440,C331,L16,L123,L122 Add EMI-1(unstuff)	13,17 29,33 35	1.0
23	Modify signal that GPU to VGA connector	R1001.2 -> SVDCCCL R1005.2 -> SVDCCDA	24	1.0
24	Reserve GPU Back Light control pull down resistor	Add R610(unstuff),R611,R612	41	1.0
25	Add polyswitch at USB connector power pin	Add FS11 between JTOUCH1.1 and VCC5_P	23	1.0
26	Disable GPU's VGA function	Del C3570 , add R377(10K) Unstuff : L34,C3568,C3569,C3571,R525	40	1.0
27	Change PWM IC for VR-HOT function	U9 -> I32-539270C-005	30	1.01
28	Change VR-HOT function	R182 -> 1.15Kohm (R11-1151T12-W08)	30	1.01